Electro-thermal Modeling of Modern Power Devices for Studying Abnormal Operating Conditions

Wu, Rui

Publication date:
2015

Document Version
Publisher's PDF, also known as Version of record

Electro-thermal Modeling of Modern Power Devices for Studying Abnormal Operating Conditions

by

Rui Wu

A Dissertation Submitted to
the Faculty of Engineering and Science at Aalborg University
in Partial Fulfillment for the Degree of
Doctor of Philosophy in Electrical Engineering

December 2015
Aalborg, Denmark

Aalborg University
Department of Energy Technology
Pontoppidanstraede 101
Aalborg East, DK-9220
Denmark
Phone: +45 29 63 20 67
Fax: +45 98 15 14 11
http://www.et.aau.dk

Printed in Denmark by Uniprint
First Edition (October 2015)
Second Edition (December 2015)

Public Defence of PhD Dissertation

Thesis Title:

Electro-thermal Modeling of Modern Power Devices for Studying Abnormal Operating Conditions

Ph.D. Defendant:

Rui Wu

Supervisor:

Prof. Frede Blaabjerg

Co-Supervisor:

Prof. Francesco Iannuzzo

Assessment Committee:

Prof. Chen Zhe (Chairman)

Department of Energy Technology
Aalborg University
Pontoppidanstraede 101
9220 Aalborg, Denmark

Prof. Alberto Castellazziä

Nottingham University
17, Clumber Court, Clumber Crescent South
NG7 1EE Nottingham, UK

Dr. Muhammad Nawaz

ABB
Forskargränd 7
721 78 Västerås, Sweden

Defence Date and Place:

Monday, December 14, 2015
Pontoppidanstraede 101, Room 23, Aalborg University

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Preface

This thesis is a summary of the PhD project "Multi-Physics Based Modeling of Power Electronic Components and Circuits". The PhD project is supported by the Center of Reliable Power Electronics (CORPE), and Department of Energy Technology at Aalborg University. Acknowledgements are given to the above mentioned institutions, as well as Otto Mønsteds Fond, which provides financially support for the conference participation and the study abroad.

This project was supervised by Professor Frede Blaabjerg, Professor Francesco Iannuzzo, and Associate Professor Huai Wang from Department of Energy Technology in Aalborg University. I would like to express my deepest gratitude to my supervisor, Professor Frede Blaabjerg, for his inspired proposals, constructive discussions, patient guidance and consistent encouragements. Furthermore, I would like to sincerely acknowledge Professor Francesco Iannuzzo for his inspired suggestions and invaluable help to both of my research and career. I would also appreciate Associate Professor Huai Wang for his continuous support and help during the whole PhD study.

This project was done with a close collaboration with the companies, such as Vestas, Danfoss, Grundfos, and KK wind solutions. I would like to send my special thanks for their support and suggestions.

I would like to express my gratitude to the honoured preliminary examiners of this doctoral dissertation, Professor Chen Zhe from Aalborg University, Professor Alberto Castellazzi from Nottingham University and Dr. Muhammad Nawaz from ABB, for their time and effort in evaluating my work.

I appreciate the fruitful collaborations with Miss Paula Diaz Reigosa, Mr. Pramod Ghimire, Dr. Kristian Bonderup Pedersen, Dr. Liudmila Smirnova as well as all the group members in CORPE. I also want to thank my colleagues from the Department of Energy Technology for the friendly environment and enthusiastic help. I would like to send my best wishes to my friends – Dao Zhou, Yongheng Yang, Xiongfei Wang, Ke Ma, Fan Zhou, Zi'an Qin, Dan Wu,Wenli Yao, Casper Jørgensen and Anna Miltersen. Moreover, my special appreciations are extended to John K. Pedersen, Tina Larsen, Mette Skov Jensen, Corina Busk Gregersen, Ann Louise Henriksen, Walter Neumayr, Mads Lund and Jan Krogh Christiansen for their assistance in many different ways.

Special thanks to my parents for their continuous encouragement and support throughout my life.

Finally, I would like to thank my wife Qian Shi for her love and support. Without your support this thesis would not have been possible.

Rui Wu

October, 2015
Aalborg Øst, Denmark

Abstract

In modern power electronic systems, there are increasing demands for improvement of the whole system endurance and safety level while reducing manufacturing and maintenance costs. Insulated Gate Bipolar Transistor (IGBT) power modules are the most widely used as well as most critical power devices in industrial power electronic systems in the power range above 10 kW. The failure of IGBTs can be classified as catastrophic failures and wear out failures. A wear out failure is mainly induced by accumulated degradation with time, while a catastrophic failure is triggered by a single-event abnormal condition, for example overvoltage, overcurrent, overheating, and cosmic rays. The degradation and wear out failure of IGBTs can be monitored by Prognostics and Health Management methods; however, it is more difficult to predict the catastrophic failure, for instance the short circuit conditions. The objective of this project has been to model and predict the electro-thermal behavior of IGBT power modules under abnormal conditions, especially short circuits.

A thorough investigation on catastrophic failure modes and failure mechanisms of modern power semiconductor devices, including IGBTs and power diodes, has been given in Chapter 2. The failure mechanisms investigation suggests that the abnormal junction temperature or hot spots normally happen with the occurrence of failure. The practical challenges in predicting junction temperature during short circuit operations are also identified: a) electro-thermal coupling effects become significant in high current and high temperature variation conditions; b) uneven current distribution and thermal loading inside the IGBT chip as well as among the different chips in an IGBT module during high dynamics of short circuit; c) there is still a lack of methods to measure the IGBT junction temperature precisely in a time duration of several or tens of μs in order to protect the devices.

According to the aforementioned investigations, a PSpice-Icepak co-simulation method is proposed to be used for studies in this thesis, which is introduced and discussed in Chapter 3. It combines a physics-based, device-level, distributed PSpice model with a thermal Finite-Element Method (FEM) simulation, gaining the possibility to take into account the electro-thermal coupling effects and uneven electro-thermal stresses among the chips. Case studies on the new and degraded modules, as well as geometrical pa-

rameters variations, further prove the effectiveness of the proposed approach in Chapter 4. Then, a 1.1 kV/ 6 kA non-destructive testing facility is built up at the Center of Reliable Power Electronics (CORPE), Aalborg University, to experimentally verify the simulation results of IGBT power modules as described in Chapter 5. The setup provides also the capability to study the wide-band-gap devices short circuit behavior in the future.

It is found that catastrophic failure is the shortfall of the reliability of modern power devices, while its behavior is difficult to be predicted. The proposed PSpice-Icepak electro-thermal co-simulation method demonstrates the capability of predicting IGBT power modules electro-thermal stresses during short circuits, which can be used for further optimizing the performance of modules.

Danske Resume

I moderne effektelektroniske systemer, er der stigende krav til at forbedre hele systemets udholdenhed og sikkerhedsniveau, mens produktions- og vedligeholdelsesomkostninger reduceres. Insulated Gate Bipolar Transistor (IGBT) effektmoduler er de mest udbredte samt mest kritiske effektenheder i industrielle effektelektroniske systemer i området over 10 kW. IGBT fejl kan generelt klassificeres som katastrofale fejl og udmattelses fejl (fatigue failure) or nedslidnings fejl (wear out failure). En nedslidningsfejl er hovedsageligt induceret af akkumuleret nedbrydning med tiden, mens en katastrofal fejl udløses af en enkelt begivenhed unormal tilstand, for eksempel overspænding, overstrøm, overophedning og kosmiske stråler. Nedbrydnings og nedslidnings fejl af IGBTs kan overvåges ved prognosticerings og sundhedsledelses metoder. Det er imidlertid vanskeligere at forudsige katastrofale fejl, f.eks kortslutningsforhold. Formålet med dette projekt har været at modellere og forudsige den elektro-termiske opførsel af IGBT effektmoduler under unormale forhold, især kortslutninger.

En grundig undersøgelse af katastrofale fejltilstande og mekanismer i moderne effekthalvlederkomponenter, herunder IGBT'er og effekt dioder, der er givet i kapitel 2. Brudmekanismens undersøgelse tyder på, at abnorm knudepunktstemperatur eller hot spots normalt sker med forekomsten af fejl. De praktiske udfordringer i at forudsige knudepunktstemperaturen under kortslutningsdrift er også identificeret: a) elektrotermiske koblingseffekter bliver betydelige i høje strøm og høje temperatuerudsvings forhold; b) ujævn strømfordeling og termisk belastning inde i IGBT-chippen samt mellem de forskellige chips i en IGBT-modul under høje dynamikker ved kortslutning; c) der er stadig mangel på metoder til måling af IGBT'ens knudepunktstemperatur præcist i en tidsvarighed af få mikrosekunder med henblik på at beskytte enhederne.

Ifølge de nævnte undersøgelser, foreslås en PSpice-Icepak co-simulering metode, der skal bruges til studierne i denne afhandling, som introduceres og diskuteres i kapitel 3. Den kombinerer en fysik baseret, enhedsniveau, distribueret PSpice model med en termisk Finite-Element Method (FEM) simulering, der giver mulighed for at tage hensyn til de elektrotermiske koblede effekter og ujævne elektrotermiske belastninger blandt chips. Casestudier om de nye og slidte moduler samt geometriske parametre variationer, yderligere beviser effektiviteten af den foreslåede tilgang i kapitel 4. Derefter, en 1,1 kV

/ 6 kA ikke-destruktiv test facilitet er bygget op på Center of Reliable Power Electronics (CORPE), Aalborg Universitet, for eksperimentelt at kontrollerede simulerede resultater af IGBT effekt moduler som beskrevet i kapitel 5. Opsætningen giver også mulighed for at studere bredt båndgabs enheders kortslutning adfærd i fremtiden.

Det konstateres, at katastrofal fejl er den største begrænsning af pålideligheden af moderne effektenheder, men er samtidig svær at forudse. Den foreslåede PSpice-Icepak elektro-termisk co-simulering metode demonstrerer evnen til at forudse IGBT effekt-modulers elektriske og termiske belastninger under kortslutninger, som kan anvendes til yderligere optimering af modulets ydeevne.

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Chapter 1

Introduction

This chapter presents the background and the motivation of the thesis, followed by the aims of the project, the outline of the thesis, and the list of the publications during the thesis work.

1.1 Background and Motivation

1.1.1 Reliability of Modern Power Devices

Nowadays, power electronics play a more and more important role in motor drives, utility interfaces with renewable energy sources, power transmissions, electric or hybrid electric vehicles and many other applications. In the most newly installed wind turbine systems [1], full-scale power converters have been adopted to interconnect the stator windings of generator and the power grid, as shown in Figure 1.1(a). Such configurations can eliminate the use of slip rings, or even gearbox and provide full power and speed controllability as well as the grid support ability. Also in the recent grid-connected Photovoltaic (PV) systems (shown in Figure 1.1(b)), the full-scale power converter has been used to remove the bulk and expensive transformer and to improve the efficiency [2]. Meanwhile, there are increasing demands for improvements in endurance and reliability of the modern power electronic systems, while reducing the manufacturing and maintenance costs [3].

Normally modern power electronic systems consist of passive components (e.g., capacitors, inductors, and resistors), connectors (e.g., bus bars), semiconductors and the corresponding drivers, and other auxiliary devices, among which the semiconductors are the key devices for switching the current and converting the power. According to a survey based on the feedback of questionnaires from manufacturers [4], 34% of the manufacturers consider power semiconductor devices are the most frangible components

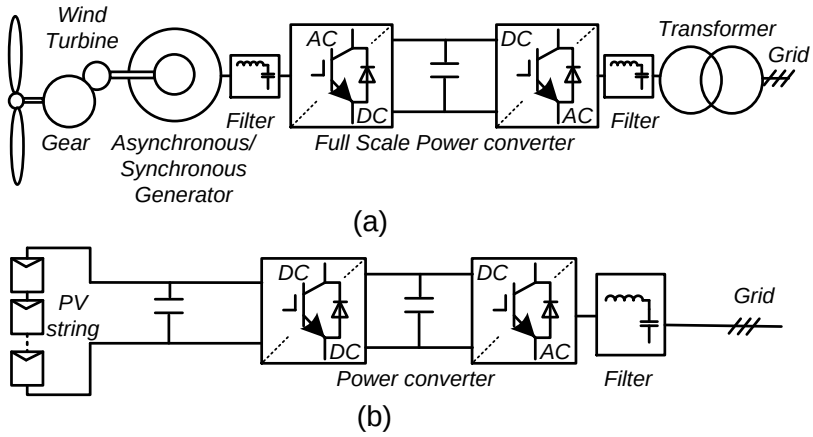

Figure 1.1: *Applications with modern power electronic systems: (a) wind turbine system with full-scale power converter; (b) transformer-less single-phase grid-connected PV system.*

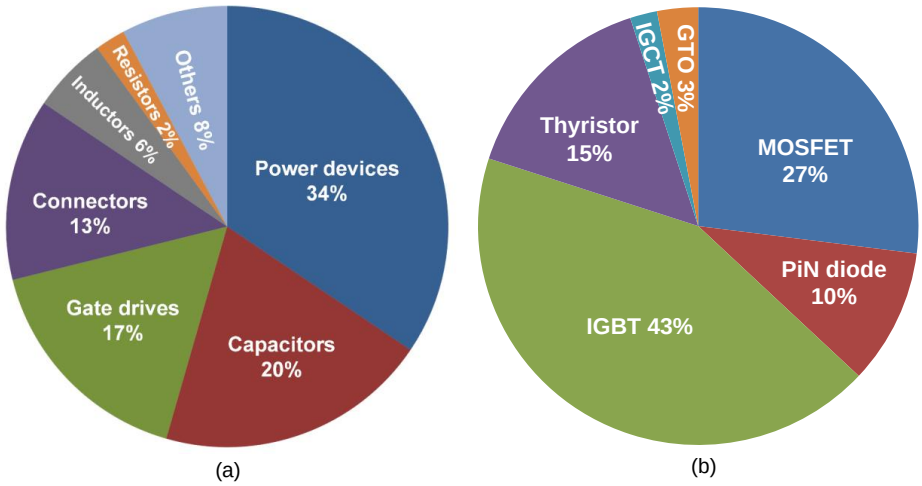

Figure 1.2: *An industry survey on power electronic systems: (a) percentage of the response to the most frangible components; (b) percentage of the response to the most used power devices question (% may vary for different applications and designs).*

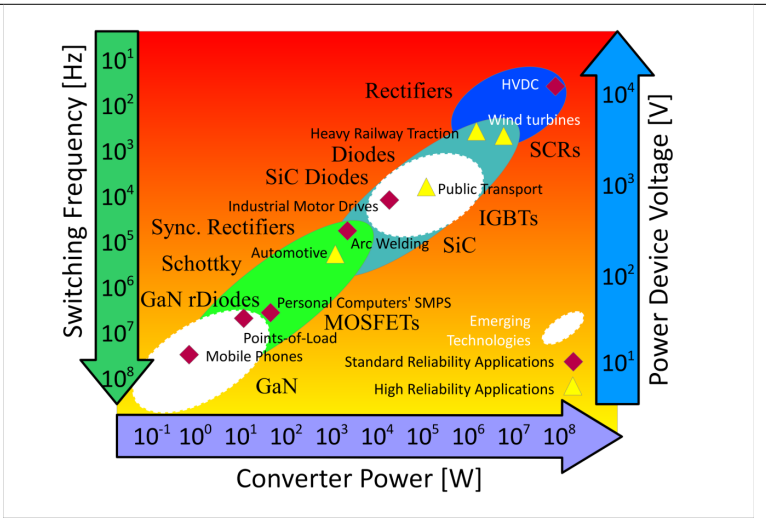

Figure 1.3: *Modern semiconductor devices and their typical applications.*

in their power electronics products (Figure 1.2(a)). Therefore, it is highly demanded to further improve the reliability of the devices.

Modern semiconductor devices can mainly be subdivided into three families: Silicon Controlled Rectifiers (SCRs), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFETs) and Insulated Gate Bipolar Transistors (IGBTs). With the development of new technologies, silicon carbide (SiC) MOSFETs/ Junction Field - Effect Transistors (JFETs) and Gallium Nitride (GaN) Heterojunction FETs (HFETs) are emerging; meanwhile older devices like Gate-Turn-off Thyristor (GTO) are replaced with Integrated Gate Commutated Thyristor (IGCT). Figure 1.3 further illustrates the semiconductor devices and their typical applications [5]. Based on the recent survey on manufacturers, IGBTs are the most widely used as well as most reliability-critical power devices in industrial power electronic systems in the range above 300 V and 10 kW (Figure 1.2(b)). The typical IGBT applications include automotive, arc welding, industrial motor drives, public transport, heavy railway traction, PV, wind turbines, voltage-source-converter high voltage direct current transmission lines, and so on.

In order to enhance the semiconductor's reliability level, the root-cause failure mechanism analysis and how to avoid failures are becoming more and more important in the recent reliability research [6]. The power devices failure analysis research can be organized around 3 generic root cause failure categories which are: errors and excessive variation, wear out mechanisms and overstress mechanisms [7]. Errors and excessive variation issues comprise the infant mortality [8], which covers every aspect of design, supply chain, and manufacturing processes. Wear out mechanisms (i.e., accumulated degradation with time), induces the wear out failures. Single-event overstress, for in-

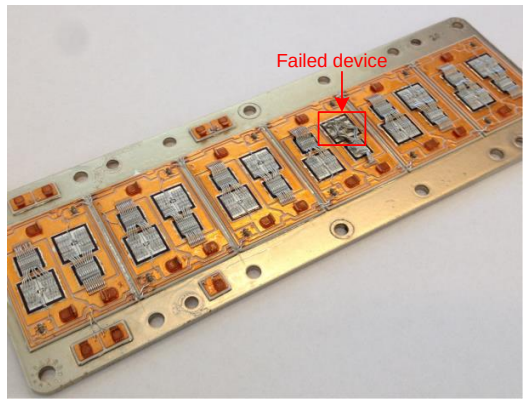

Figure 1.4: *The photo of a failed IGBT power module due to short circuit.*

stance overvoltage, overcurrent, overheating, cosmic rays and so on, can trigger the catastrophic failures.

Reliability improvements on errors and excessive variation can be done by implementing error proofing and proper manufacturing process control to ensure robustness [9]. The degradation and wear-out failures of semiconductors can be monitored by different Prognostics and Health Management (PHM) methods. It is also worth noting that PHM methods are not always feasible in practical applications due to the increase of design cost [10]. On the contrary, it is more difficult to predict the catastrophic failures, as well as to quantify the aging effects of the power devices due to abnormal operations. Particularly, the short circuit operation is critical to semiconductors, where both high voltage and current are applied so that the high power dissipation can lead to a destruction in a few microseconds, as illustrated in Figure 1.4. Moreover, the power devices' short circuit operation is also fatal to power converters, because the uncontrolled short circuit current may destroy the other components in the system quickly [11]. It is worth pointing out the junction temperature (Tj) is probably the most critical parameter responsible for IGBT catastrophic failures. For instance, the phenomena of current concentration and thermal runaway, which causes IGBT failures during heavy loads and short circuits, are commonly connected with regenerative effects involving high junction temperature. Additionally, the final destruction coming from various failure-triggering events, (e.g., dynamic breakdown, latch-up and gate driver failure) is due to high junction temperature [12].

1.1.2 Summary of the Package-related Failure Mechanisms

The reliability of semiconductor devices is closely related to the package. There are different package types based on the power range of the semiconductor devices, for instance

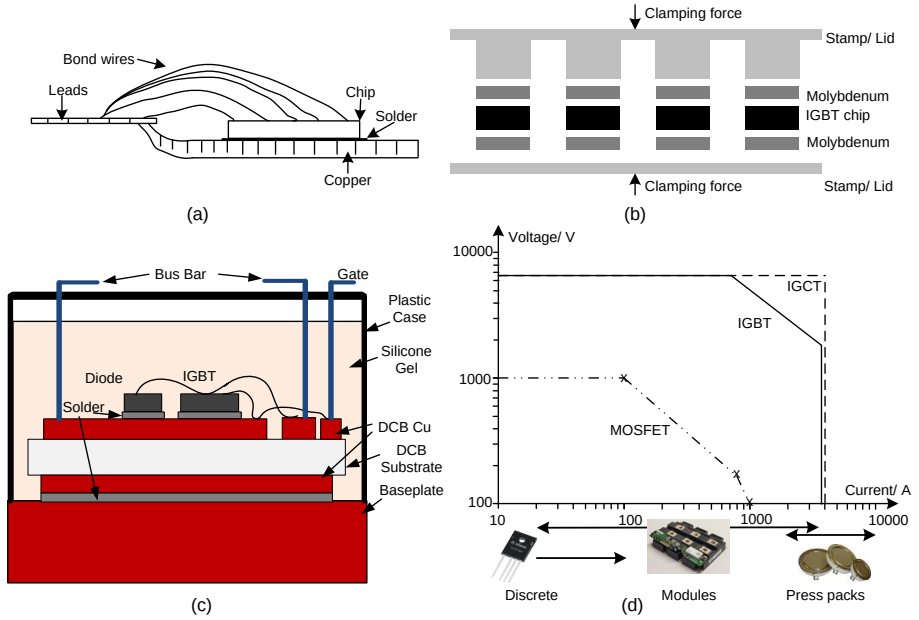

Figure 1.5: *Different power devices packaging technology: (a) internal structure of discrete IGBT device; (b) cross section of IGBT press-packs; (c) cross section of IGBT power modules; (d) power range of modern semiconductor devices together with the predominant package type.*

discrete packages, power modules and press-packs. For the low power and low blocking voltage devices, discrete packages (such as the Transistor Outline (TO) package) are most common, where the chip is soldered directly to a solid copper base, as displayed in Figure 1.5(a). For high blocking voltage and high power rating devices (i.e., more than 10 A and 1200 V), the power module is the dominating package, which is in particular characterized by an electrically insulated architecture – the semiconductor chips are electrically insulated from the heat dissipating mounting surface (e.g., heat sink). Press-packs are applied for the even higher power range than power modules, where semiconductor device is mounted between two metal discs in order to homogenize the pressure [11]. The cross sections of the typical press-pack and power module structure are illustrated in Figure 1.5(b) and (c) respectively. It is worth mentioning that there are some new packaging designs based on the above traditional packages. For instance, IXYS has proposed the discrete packages with Direct Copper Bonded (DCB) layers [13]. Fairchild has developed DCB substrate-based molded power modules [14]. ABB has proposed StakPak modules [15], which are press-packs packaging with individual press-pins

for each of the parallel connected chips.

Table 1.1: *Comparison between power modules and press-packs packages.*

	Power Modules	**Press-packs**
Advantages	Electrical insulation	Compact design
	Lower cost, mass volume,	Double side cooling
	Easy maintenance	No emitter bond-wires
	Multiple configurations	High power density
Disadvantages	Low thermal performance	No electrical insulation
	Complicated structure	Higher cost
	Low power density	Maintenance difficulty

The power module has a wider range of applications because of its low cost and easy mounting and maintenance requirements [11]. Another advantage is that the internal semiconductors can be configured to obtain multiple functions (e.g., half-bridge configuration, three-phase converter). However, due to the soldering and bond-wire connection of internal chips, the power modules may also suffer from poor thermal behavior, lower power density, and higher failure rates. The press-packs connect the parallel chips by direct press-pack contacting (for instance springs), which can improve the reliability level, obtain higher power density (easier stacking for series connection), and better cooling capability. A comparison of the advantages and drawbacks between the power modules and press-packs is given in Table 1.1. Based on a survey of the packages and their power ranges in Figure 1.5(d), it can be seen that in the medium and high power applications, the most prevalent package is the power module.

There are plenty of research on the package-related failure mechanisms of both press-packs and power modules. Figure 1.5(b) displays the internal construction of a conventional IGBT press-pack in a simplified schematic view. The IGBT chip is placed between the metal plates in a hermetically sealed capsule, electrical and thermal contact are established by the application of force. A distribution board inside the press-pack connects the parallel IGBT chips gate through a corner pad. The ABB StakPak technology [15] represents individual press-pins to ensure correct pressure for all of the parallel connected chips in the press-packs. Press-pack IGBTs contain no bond wires or solder joints at all, and the contact to the gate, collector and emitter is made through pressure contact. Hence, the common failure modes of press-packs are fretting damage, spring fatigue, spring stress relaxation, which is mainly caused by the Coefficients of Thermal Expansion (CTE) mismatch between the different layers of materials [16].

Figure 1.5(c) presents the cross section of typical IGBT power modules. The module exterior consists of a plastic frame with screw connections and a metallic baseplate. The plastic frame should be mechanically stable, and have high tensile strength within the whole temperature range. It must also be electrically insulating, and ensure a long

creepage distance at its surface. The silicone gel has very good electrical insulation properties. Most high-power IGBT modules have a copper baseplate to provide fine thermal connection to the cooling medium. The DCB-substrate consists of a ceramic dielectric insulator with copper bonded to it. The DCB provides electrical insulation between the potential of the power devices and the potential of the heat sink. It is also important that the DCB provides good thermal connection to the heat sink. The upper copper layer of the DCB consists of copper tracks. The metallic backside of the IGBT chip, the collector side, is soldered directly onto these copper tracks. Bond wires on the top of the chip provide electrical connection to the gate and emitter contact of the chip. Aluminum (Al) bond wires are the most common, and the number of bond wires is determined by the rated current of the module.

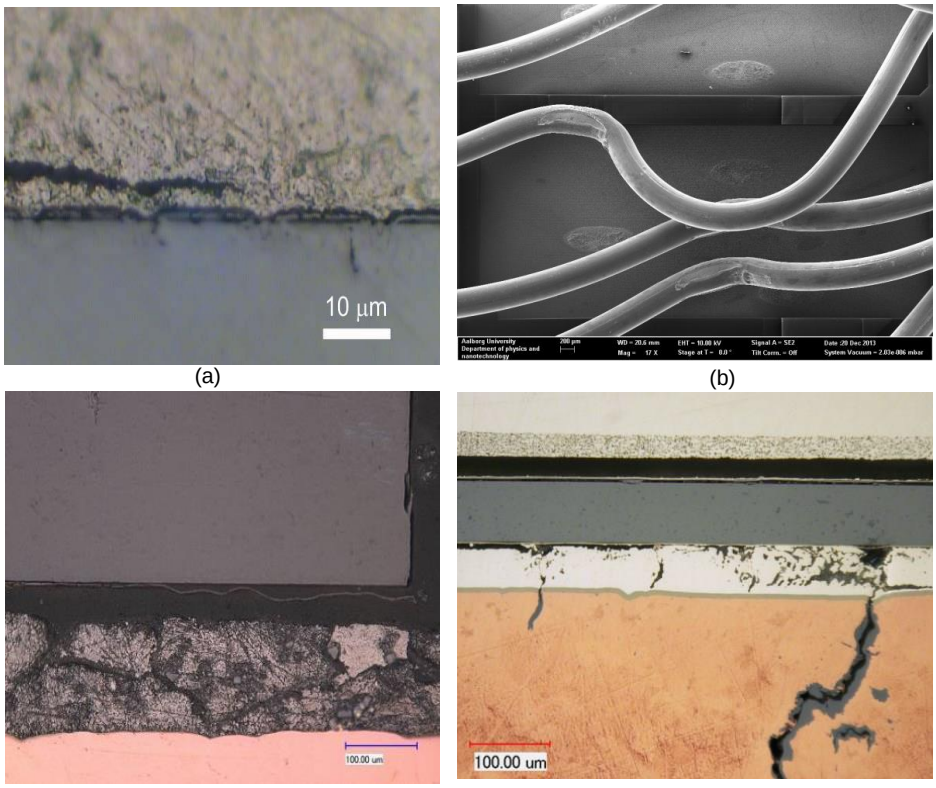

Figure 1.6: *Selected failures of semiconductor power devices: (a) bond wire heel cracking, (b) bond wire lift-off, (c) solder degradation, (d) vertical cracks in the substrate metal.*

The common wear-out failure mechanisms of the IGBT power modules are bond wires lift-off, heel cracking, solder joint fatigue, and Al reconstruction [16]. Bond wires fatigue (mainly lift-off and heel cracking,as shown in Figure 1.6(a)(b) [17]) is due to the CTE mismatch between the Al bond wire and the silicon chip [18]. Because bond wires are exposed to the full temperature swing caused by the chip power dissipation and their own ohmic self-heating, shear stress and repeated flexure can be generated, and hence fatigue may happen. Similar mechanism can lead to solder joint fatigue (e.g., cracks, voids, and delamination, as shown in Figure 1.6(c)(d) [19]) between the chip and ceramic substrate, or between the ceramic substrate and base plate. Aluminum reconstruction is mainly caused by the different CTEs of the aluminum layer and the semiconductor chip, which reduces the effective cross-section of the metallization and results into an increase of the aluminum layer sheet resistance and the collector-emitter saturation voltage $V_{ce,sat}$ with time [20]. Further improvements of the power modules reliability level is one of the most exciting and important challenges for engineers. The main trends to improve the packaging technology of IGBT modules are to introduce pressure contact for eliminating the base plate and thus base plate soldering, sintering technology to avoid the chip soldering, as well as replaced bond-wire material to reduce the coefficient of thermal expansion— to increased lifetime of IGBT power modules, as reported in [21], [22].

However, most prior research focuses on the wear-out failure mechanisms and how to prolong the power module lifetime by proper design, while much less attention has been addressed to catastrophic failure mechanisms. In particular, the electrical and thermal behavior of IGBT power module under abnormal conditions is still missing. The Center of Reliable Power Electronics (CORPE) in Energy Department of Aalborg University is oriented to identify and solve these power electronics reliability issues.

1.1.3 Project Motivation

The reliability of power electronics can be improved by different methods [23]: studying the physics of failure and failure mechanisms; evaluating the reliability level from constant failure rate to failure level with time; introducing the state-of-the-art methodologies in the area of microelectronics reliability to the area of power electronics; adding more intelligent control and monitoring, as illustrated in Figure 1.7.

Different packaging methods have been proposed for the aforementioned purpose, and consistent improvements are achieved to extend the lifetime of the power semiconductors. Comparing with the degradation and wear-out failure caused by normal operations, the catastrophic failure induced by single-event overstress (e.g., short circuit) is more difficult to be predicted and protected due to the high electrical and thermal stress (exceeding the specifications) or dynamics within the short time duration (in μs or ms level). It should be pointed out that it is challenging to experimentally study the catastrophic failure because of the safety requirements, as well as the risk of destroying

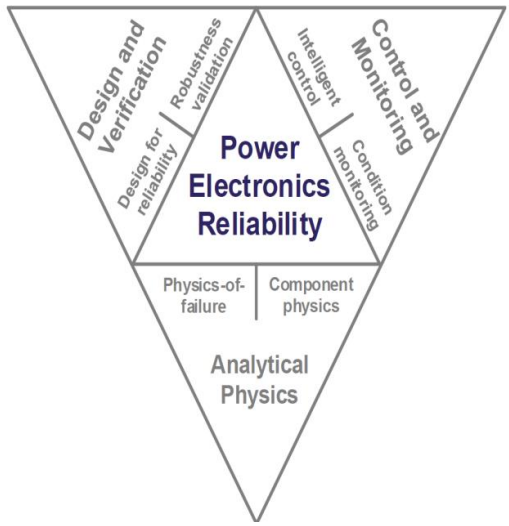

Figure 1.7: *The scope of reliability of power electronics.*

the device. Nevertheless, those high dynamics phenomena can be immensely and deeply investigated by means of multi-physics modeling methods, and by which the reliability phenomenon can be further explained.

The above considerations have initiated the present research project. In summary, the major motivation of this project is to model and simulate the electrical and thermal behavior of modern power semiconductors under abnormal conditions in order to understand the corresponding failure mechanism, and thus to reveal the ageing impacts on devices characteristics to provide a protection guideline and to improve the robust level in the future reliability-critical power electronic applications.

1.2 Aims of the Thesis

1.2.1 Scientific Questions

This PhD project tries to answer: how do the modern power semiconductors electrically and thermally behave under abnormal operating conditions. For this aim, there are some crucial questions that need to be answered in an explicit way:

- *What is the electro-thermal coupling effect in high current and high temperature variation abnormal conditions in power modules?*
- *How will the degraded semiconductors behave under abnormal operating conditions? What are the ageing effects (bond-wires lift-off, threshold voltage degradation) on*

IGBT behavior under abnormal conditions?

- *What is the imbalance current distribution and thermal loading inside the IGBT chip during the high dynamics? Additionally, what about the case in the multi chips power modules?*
- *What is the chip temperature level during the extreme abnormal conditions? Is there any method to measure the junction temperature in the time duration of several or tens of μs?*

1.2.2 Objectives

With the aforementioned research questions, the primary goal is to develop a physics-based electro-thermal method for evaluating semiconductors performance under abnormal conditions, and then apply it in study cases of power modules under different status. Consequently, the secondary goal is to establish an experimental setup for evaluating the studied power modules under abnormal conditions. The objectives of this project are listed below in details:

Physics-based Electro-thermal Simulation Method of IGBT Power Modules-

This study is aimed to simulate the modern power semiconductors electrically and thermally under abnormal conditions. Physics-based electro-thermal methods and tools for evaluating and improving the critical performances under short circuits will be established; where the electrical and thermal stresses of the IGBT power modules are the main focus.

Experimentally Evaluate IGBT Power Modules under Abnormal Conditions-

In order to guarantee a correct evaluation of the proposed method, a non-destructive testing facility will be constructed with the capability of repetitively and safely testing MW-level IGBT power modules.

1.2.3 Research Scopes and Limitations

In this project, commercial 1.7 kV/1 kA IGBT modules are considered in various case studies, which are widely used in high power applications. There are two typical short circuits for IGBT: the Type I short circuit happens during turn-on, and the Type II happens when IGBT is on-state. The performance of the Type I short circuit is more closely related to the characteristics of the specific devices. Therefore, all the simulations and experiments focus on Type I short circuit in the study.

The proposed electro-thermal methods can later be adopted for different power devices, yet adaptations and modifications might be necessary with corresponding Spice models and geometry information. It can be easily applied to other types of IGBT packages (for instance, discrete and press-pack devices) with the updated packaging geometry information. All the short circuit experiments are performed by means of the Non-Destructive Tester (NDT) developed at CORPE, Aalborg University.

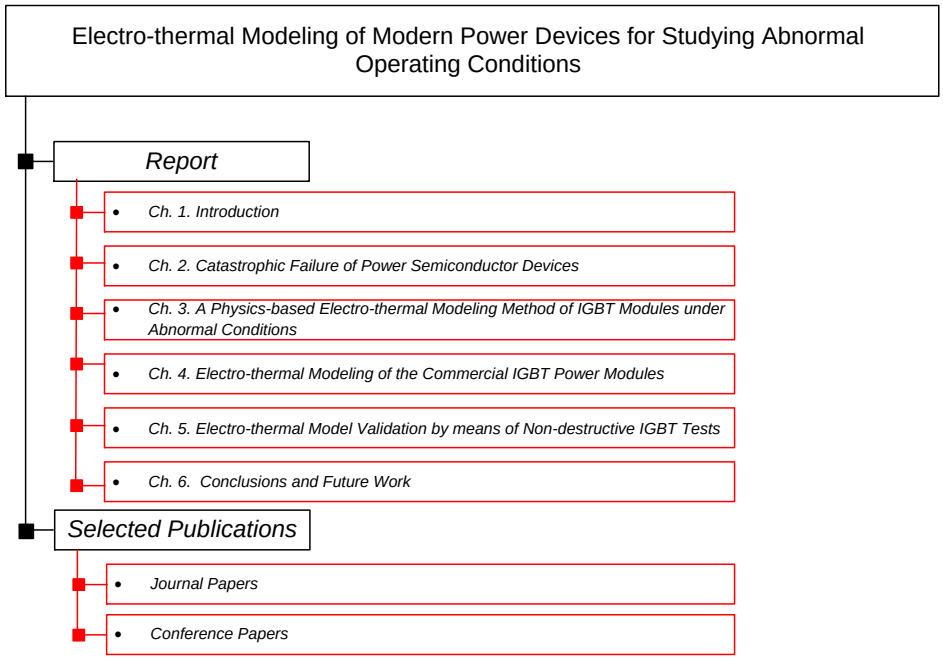

Figure 1.8: *Thesis structure and the studied topics.*

1.3 Outline of the Thesis

This thesis consists of two parts: Part I – Report and Part II – Publications. Part I is a summary report of the work done throughout the Ph.D. study and contains 6 chapters. Figure 1.8 gives an overview of the thesis structure and research topics. The structure of the thesis is organized as follows:

Chapter 1 presents the background and motivation of this research. Furthermore, the aims, objectives and structure of the thesis are also addressed.

Chapter 2 gives a thorough overview on catastrophic failure modes and failure mechanisms of modern power semiconductor devices, including IGBTs and power diodes. Then the IGBT short circuit failure mechanism is described in more detail. Practical challenges of predicting the IGBT electro-thermal behavior during short circuit operations are also identified.

Chapter 3 proposes a physics-based PSpice-Icepak co-simulation method to study the temperature effects. It combines a physics-based, device-level, distributed PSpice model with a thermal Finite-Element Method (FEM) simulation, gaining the possibility to take into account the electro-thermal coupling effects and uneven electro-thermal

stresses among chips. Case studies on one section of the commercial 1.7 kV/ 1 kA IGBT power modules are given for both new and degraded conditions (e.g., bond-wire lift-off and threshold voltage degradation devices).

Chapter 4 applies the proposed co-simulation method to multi-chips IGBT power modules. Through case studies on 1.7 kV/1 kA IGBT power modules, the co-simulation tool successfully predicts the short circuit current sharing among the paralleled IGBT chips.

Chapter 5 validates experimentally the simulation results from Chapter 3 and Chapter 4, which proves the effectiveness of the proposed approach. The 1.1 kV/ 6 kA rated non-destructive testing facility is described, which has been built up for high power IGBT module short circuit tests. Both the simulated electrical behavior and the thermal performance during short circuits have been verified.

Chapter 6 discusses the conclusions, highlights of the thesis and some research proposals for the future work.

1.4 List of Publications

A list of the papers derived from the Ph.D. project, which have been published, is given as follows:

Journal Papers

I. **R. Wu**, F. Blaabjerg, H. Wang, Huai, and M. Liserre, "Overview of catastrophic failures of freewheeling diodes in power electronic circuits," *Microelectronics Reliability*, vol. 53, no. 9-11, pp. 1788–1792, Sept. 2013.

II. **R. Wu**, P. D. Reigosa, F. Iannuzzo, L. Smirnova, H. Wang, and F. Blaabjerg, "Study on Oscillations during Short Circuit of MW-scale IGBT Power Modules by means of a 6 kA/1.1 kV Non-Destructive Testing System," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 3, pp. 756-765, Sept. 2015.

III. P. D. Reigosa, **R. Wu**,F. Iannuzzo, and F. Blaabjerg, "Robustness of MW-Level IGBT modules against gate oscillations under short circuit events," *Microelectronics Reliability*, vol. 55, no 9-10, pp. 1950-1955, Aug.-Sept. 2015.

Conference Papers

I. **R. Wu**, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic Failure and Fault-Tolerant Design of IGBT Power Electronic Converters - An Overview," in *Proceedings of the 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, pp. 507-513, 2013.

II. **R. Wu**, F. Iannuzzo, H. Wang, and F. Blaabjerg, "Fast and accurate Icepak-PSpice co-simulation of IGBTs under short-circuit with an advanced PSpice model," in *Proceedings of 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, pp. 1-5, 2014.

III. **R. Wu**, F. Iannuzzo, H. Wang, and F. Blaabjerg, "An Icepak-PSpice Co-Simulation Method to Study the Impact of Bond Wires Fatigue on the Current and Temperature Distribution of IGBT Modules under Short-Circuit," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.5502-5509, 2014.

IV. **R. Wu**, H. Wang, K, Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A Temperature-Dependent Thermal Model of IGBT Modules Suitable for Circuit-Level Simulations," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2901-2908, 2014.

V. **R. Wu**, L. Smirnova, F. Iannuzzo, H. Wang, and F. Blaabjerg, "Investigation on the Short-circuit Behavior of an Aged IGBT Module through a 6 kA/1.1 kV Non-Destructive Testing Equipment," in *Proceedings of the 40th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp. 3367-3373, 2014.

VI. L. Smirnova, J. Pyrhönen, F. Iannuzzo, **R. Wu**, and F. Blaabjerg, "Round busbar concept for 30 nH, 1.7 kV, 10 kA IGBT non-destructive short-circuit tester," in *Proceedings of 16th European Conference on Power Electronics and Applications (EPE'14 ECCE Europe)*, pp. 1-9, 2014.

VII. **R. Wu**, F. Iannuzzo, H. Wang, and F. Blaabjerg, "Non-Destructive Investigation on Short Circuit Capability of Wind-Turbine-Scale IGBT Power Modules," in *Proceedings of the Wind energy Grid-Adaptive Technologies (WeGAT)*, pp. 1-6, 2014.

VIII. Z. Hu, **R. Wu**, X. Yang, Z. Lin, and F. Blaabjerg, "A novel power control strategy of Modular Multi-level Converter in HVDC-AC hybrid transmission systems for passive networks," in *Proceedings of the 5th IEEE International Symposium on Power Electronics for Distributed Generation Systems(PEDG 2014)*, pp. 1-6, 2014.

IX. **R. Wu**, F. Iannuzzo, H. Wang, and F. Blaabjerg, "Electro-Thermal Modeling of High Power IGBT Module Short-Circuits with Experimental Validation," in *Proceedings of the 61st Annual Reliability & Maintainability Symposium (RAMS)*, pp.1-7, 2015.

X. P. D. Reigosa, **R. Wu**,F. Iannuzzo, and F. Blaabjerg, "Evidence of Gate Voltage Oscillations during Short Circuit of Commercial 1.7 kV/ 1 kA IGBT Power Modules," in *Proceedings of International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe 2015)*, pp.1-6, 2015.

XI. **R. Wu,**, L. Smirnova, H. Wang, F. Iannuzzo, and F. Blaabjerg, "Comprehensive Investigation on Current Imbalance among Parallel Chips inside MW-Scale IGBT Power Modules," in *Proceedings of the 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia 2015)*, pp. 850-856, 2015.

XII. **R. Wu**, P. D. Reigosa, F. Iannuzzo, H. Wang, and F. Blaabjerg, "Experimental Investigation on the Short Circuit Performance of MW-level IGBT Power Modules under Non-negligible Stray Inductance," in *Proceedings of the 17th European Conference on Power Electronics and Applications (EPE2015)*, pp. 1-7, 2015.

Chapter 2

Catastrophic Failures of Modern Power Semiconductor Devices

This chapter discusses the common failure modes of modern power semiconductor devices, and the catastrophic failure is highlighted. It further summarizes some typical failure mechanisms of power diodes and IGBTs. Afterwards, it gives special attentions to the IGBT short circuit mechanism and the corresponding reliability issues.

2.1 Power Semiconductor Devices Failures Classification

Most power semiconductor failures can be classified as: errors and excessive variation failure, wear-out failure, catastrophic failure according to the generic root cause, which are shown in Figure 2.1. Errors and excessive variation issues comprise the infant mortality, which covers every aspect of design, supply chain, and manufacturing processes. For example, the Electro-Static Discharge (ESD) on IGBT gate can be caused by the manufacturing assembling process [24]. Wear-out failure is mainly caused by accumulated degradation with time, which may take up to several years to occur. It usually accompanies with device parameters degradation, before a disruption happens. As discussed in Section1.1.2, semiconductor's wear-out failure modes are close related to the packages: the common wear-out failure of power modules are bond wires lift-off, heel cracking, solder joint fatigue, and Al reconstruction, while for press-packs, are fretting damage, spring fatigue, spring stress relaxation.

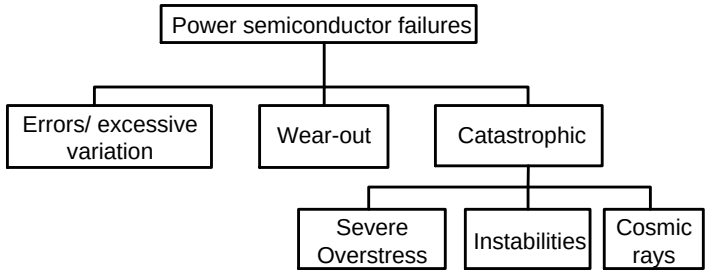

Figure 2.1: *Classification of power semiconductor devices failures.*

Catastrophic failures happen in short periods, typically in the range of microseconds or milliseconds, which often lacks of methods to predict. Catastrophic failures can be subdivided into cosmic rays induced burnout, instabilities and severe overstress. Cosmic rays induced failures have been discovered for high current, high voltage semiconductor devices (like diodes, thyristors, GTOs, IGCTs, IGBTs, etc.) in the early 1990's [25]. Cosmic rays induced burnout failures have no precursors, and IGBT is more prone to the cosmic radiation than other devices like diodes, thyristors, GTOs. Primary cosmic rays are high-energy particles (e.g., pion, muon, neutrons), which can cause Si chip breakdown at a random location. Instabilities are regenerative phenomena caused by device internal aspects, for example, internal geometries, layout, chip technology and manufacturing process [5]. Severe overstress is caused by harsh external conditions (external of the package), for instance overvoltage, overheat and short circuits.

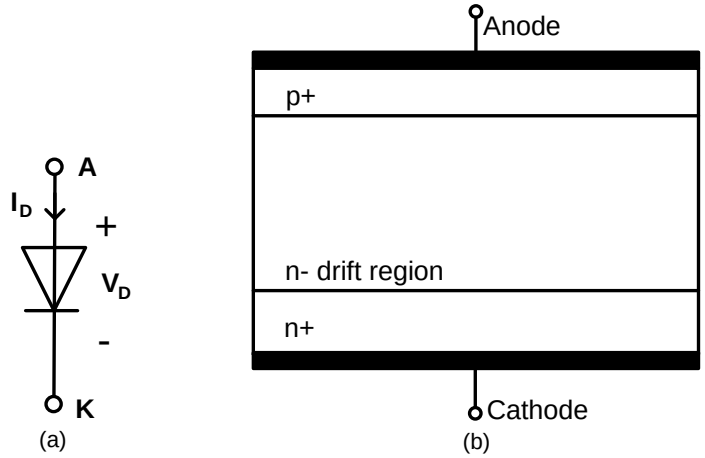

Figure 2.2: *Power diode symbol and structure: (a) circuit symbol with terminals: Anode (A), Cathode (K); (b) cross section of most widely used power diode structure.*

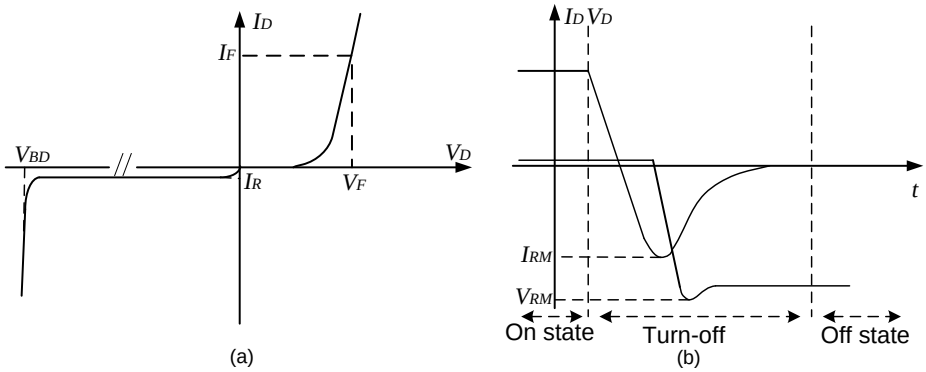

Figure 2.3: *Characteristics of power diodes: (a) I-V characteristics with parameters definitions; (b) normal turn-off waveforms.*

2.2 Power Diode Catastrophic Failure Mechanisms

2.2.1 Power Diode Structure and Operations

The power diode is a two-terminal (anode and cathode) device, and the circuit symbol is shown in Figure 2.2(a). The typical cross-section structure is illustrated in Figure 2.2(b), which contains three regions: (1) a highly doped P region (P+), connected to the anode contact; (2) a lightly doped body region (N-), also indicated as intrinsic region; (3) a highly doped N region (N+) at the back side. Thus, the power diode is also entitled as P-i-N diode in the literatures. The high voltage reverse-blocking capability is supported by the N drift region.

Power diode anode current versus voltage (I-V) curve is illustrated in Figure 2.3(a), where the anode-cathode voltage (V_D) is plotted on the horizontal axis, while the anode current (I_D) is on the vertical axis. When a positive voltage is applied to anode, the diode is forward biased, and the characteristic associates a defined current I_F to the voltage drop V_F. When a negative voltage is applied to the anode, the diode is reverse biased, and the high voltage reverse-blocking capability is supported by the N drift region. In reverse bias, V_{BD} is the physical breakdown voltage, and I_R denotes the leakage current measured at a defined reverse voltage.

Most power diode catastrophic failures happen during the diode turn off transients, which is illustrated in Figure 2.3(b). It can be noted that the current reduces to zero and goes further to negative, until reaching the peak reverse recovery current I_{RM}. This phenomenon is defined as reverse recovery, because the stored charge in the body has to be removed. Then there is a sharp increase of voltage until the peak value V_{RM}, which corresponds to an equal growth in the integral of the electric field. At last, the current decreases to zero with a smooth tail, and the reverse voltage equals to the applied

voltage.

2.2.2 Power Diode Catastrophic Failures

As generally discussed in Section 2.1, power semiconductors catastrophic failure can be classified as cosmic rays induced burnout, instabilities and severe overstress.

Cosmic rays induced failure

The failure mechanism is related to the high-energy particles [26]. When a small part of the high-energy neutrons travel through a semiconductor device, they collide with the cores of silicon atoms, and create back scattered ions, which further generate locally again a dense plasma of charge carriers. These carriers are separated in the space charge region under the blocking mode, and lead to a current pulse. If the electric field is higher than a certain threshold value – which depends on the initial plasma generation – then impact ionization creates more carriers than the carriers created by the diffusion. Then the device is flooded locally with free carriers within some hundreds of picoseconds; hence, a local current filament occurs. Finally, the very high local current density destroys the semiconductor device. The localized breakdown in the bulk of the devices is not related to junction termination instabilities, and the breakdown spot location on the wafer is random. The onset of the breakdown occurs without a precursor within a few nanoseconds and there is no sign of early failures or wear out. The failure rate is constant in time but strongly dependent on the applied voltage, operating altitude and shows a small dependence on temperature [27].

Instabilities

Freewheeling diodes are prone to have instabilities during reverse recovery process, and several typical phenomenon and mechanisms are given as follow:

Snappy recovery.

Diode snappy recovery is a phenomenon that the current declines steeply after the reverse recovery current reaches the peak value. The main reason is the sudden disappearance of the remaining carriers at the end of the recovery process. Due to high di/dt and stray inductance in the circuit, high voltage spikes can appear and damage the diode. H+ irradiation has been proposed to obtain a trade-off between diodes switching speed and softness, which can avoid snappy recovery and validated by comprehensive experiments and numerical investigations [28]. Controlled Injection of Backside Holes (CIBH) diodes are also proposed to increase the soft reverse recovery behavior [29]. It is still a critical point to avoid snappy recovery when designing freewheeling diodes.

Reverse-recovery dynamic avalanche.

Dynamic avalanching occurs at high di/dt switching speeds, which can result in the generation of a hot spot in the silicon die itself due to non-uniform current crowding, and further lead to the destruction of the device. The causes of these hot spots can range from process to material variations in a single diode silicon chip.

Impact ionization near N-N+ junction leads to a negative differential resistance and current filament, finally a thermal runaway. This process (called Egawa effect) is very similar to the second static avalanche breakdown in bipolar transistors [30]. Local heating and hot spots at the corner of anode is observed even the reverse voltage is lower than the static breakdown voltage. A detailed study of dynamical behavior of the plasma layer also explains this reverse recovery failure [31]. A merged P-i-N schottky diode is proposed to replace conventional P-i-N freewheeling diode, which shows deep $N+$ emitter and a wide n-base can improve the dynamic avalanche characteristic. CIBH diode can also prevent the filaments in N-N+ junction. Electro-thermal simulations show that thermal-induced filament can lead to destructive thermal runway and it is sensitive to contacts thermal resistance [32]. To further improve power diode robustness against this failure, chip structure can be refined and the thermal management should be enhanced.

Current Filamentation.

Current filamentation has been also considered as the main power diode failure mechanism. Experiments on 3.3 kV power diodes and the corresponding analytical and simulation studies, suggest that a stable filament of injected electrons from the N+ side could arise very quickly during reverse recovery in extreme conditions [33]. The detailed mechanism is: during very hard turn-offs (i.e., high initial current, high di/dt gradients and high voltage) the internal electric field peak can move from its normal position at the P+N- interface down to the N-N+ one. There, it can reach much easily the critical value and make avalanche injection beginning. The phenomenon results unstable (i.e., catastrophic) if the generated current by avalanche becomes equal or greater than the current flowing through the device. In this case, the device latches up and it is destroyed. This phenomenon can happen in several power devices other than the diodes, as demonstrated in [34].

Besides the above instabilities, it is worth mentioning some studies about oscillatory behaviors potentially leading to failure during reverse recovery of 3.3 kV and 4.5 kV diodes and some corresponding solutions concerning the placement of P+ islands inside the N+ cathode layer [35].

Severe Overstress

Freewheeling diodes can also suffer from the severe overstress, such as high voltage, high current and overheat:

Static high voltage breakdown.

High reverse voltage can cause diodes static avalanche. With reverse voltage reaching first the static avalanche point, the current rises with positive slope, while no permanent failure happens. If the voltage reaches the second avalanche point, there will be a Negative Differential Resistance (NDR), which will lead to current filament and a quick short circuit. Detailed numerical simulations were carried out for a rated 3.3 kV/1 kA diode, and the results are shown in Figure 2.4 [36]. The avalanche capability is strongly

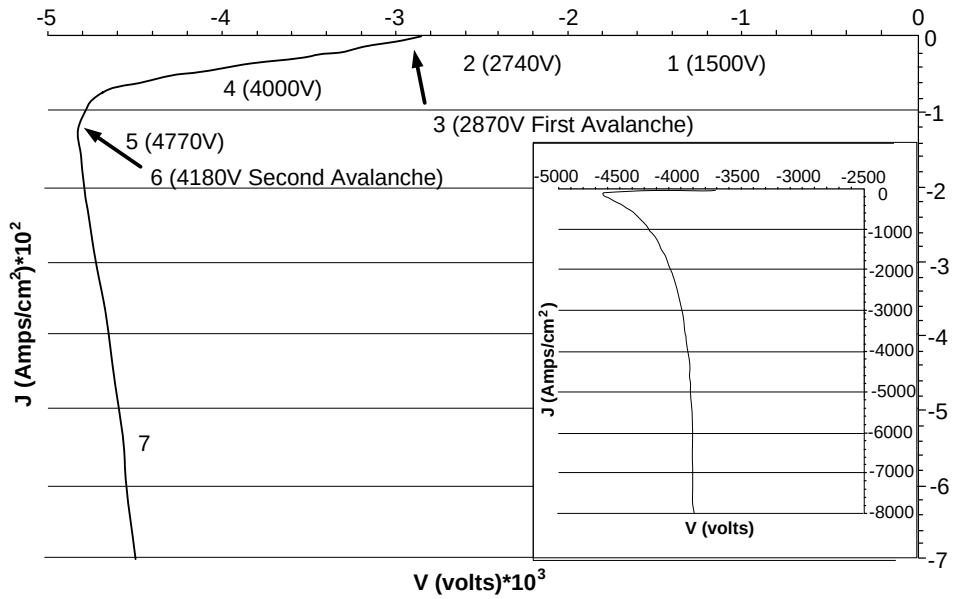

Figure 2.4: *First and second static avalanche breakdown of a 1700V rated power diode.*

dependent on the initial breakdown location and the edge termination design, and the common failure locations are near the chip's edge and near the bonding wires [37]. Since the operating voltage of freewheeling diodes is normally much lower than rated voltage, static high voltage breakdown is not common in nowadays applications.

High leakage current at high junction temperature.

The leakage current of the power diodes is usually very low, but it increases with voltage and temperature. The value is roughly doubled for every 10 °C raise of temperature. This effect is more obvious for gold-diffusion diodes, which may be thermally destroyed at high temperature. Experiments demonstrate that high temperature operations required by some modern applications like automotive can be unsafe, because they can provoke a thermal runaway involving the termination leakage current [38]. Terminations reliability at high temperature in the off state has also to be considered. The leakage current rising can also be due to repetitive electrostatic discharge [39].

2.3 IGBT Catastrophic Failure Mechanisms

IGBT is a three-terminal (gate, collector and emitter) device, and the current flow between the collector and emitter is fully controlled by the gate voltage. IGBT cir-

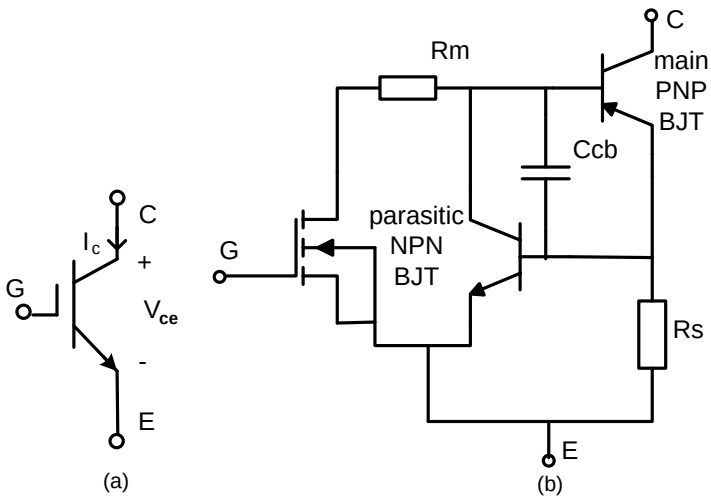

Figure 2.5: *IGBT component: (a) circuit symbol with terminals: Gate (G), Collector (C), Emitter (E); (b) equivalent circuit.*

cuit symbol is shown in Figure 2.5(a). IGBT is a hybrid bipolar-MOS device, and an equivalent circuit is illustrated in Figure 2.5(b), which contains a MOSFET, main PNP Bipolar Junction Transistor (BJT), parasitic NPN BJT, and parasitic resistance and capacitance. The main current flows through the main PNP BJT, the base current of which is fed by MOSFET drain current. Thus, the current control of BJT converts to gate voltage control of MOSFET. The parasitic NPN BJT is undesired because it may form a parasitic PNPN thyristor together with the PNP BJT, which can lead to a dangerous failure "latch-up". It should be noted that IGBTs are usually connected in anti-parallel with freewheeling diodes so that the current can flow in two directions.

2.3.1 State-of-art IGBT Structure and Operations

Because the IGBT is mainly applied in high voltage and high power application, it becomes a hot issue to decrease the IGBT power losses. The main IGBT improvements from a chip design point of view are the gate structure and doping profiles. Most widely used structures of IGBT have been Non-Punch-Through (NPT), Punch-Through (PT), and the trench-gate PT, which are illustrated as Figure 2.6(a), (b), (c) respectively.

The typical gate structures are planer gate and trench gate, which are shown in Figure 2.6(a) and Figure 2.6(c) respectively. Comparing with the planer gate, the trench gate can reduce the cell size, leading to a large increase in cell density and power density. What's more, the trench structure can better bypass the parasitic NPN BJT, thus decreasing the saturated collector-emitter voltage $V_{ce,sat}$ and avoid the dangerous "latch-up" It should be pointed out that trench gate structure also exhibits a higher

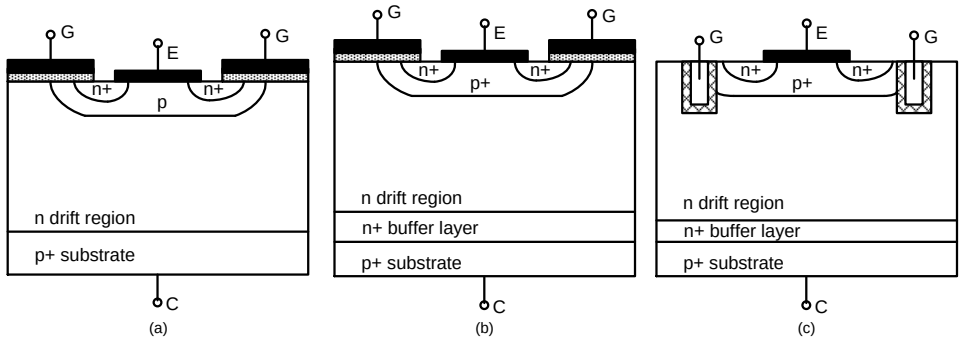

Figure 2.6: *Cross section of most widely used IGBT structures: (a) Non-Punch-Through (NPT) IGBT; (b) Punch-Through (PT) IGBT with n+ buffer layer; (c) Trench-gate with soft/light PT or field stop layer IGBT.*

transconductance, which may result in instabilities under abnormal conditions, as further addressed in Section 2.4.2.

The definition of NPT and PT are based on the electric field shape during IGBT blocking state. As shown in Figure 2.7(a), the electric field of the NPT stops at the n drift region. On the contrary, PT IGBT has an additional highly n-doped buffer layer ($n+$ layer) between the substrate and drift region: the electric field punch through the $n-$ layer into the $n+$ layer, and the field is steeper inside the $n+$ layer than $n-$ layer, as illustrated in Figure 2.7(b). This layer is sometimes referred to as the field-stop layer. The PT IGBT is thinner than NPT IGBT for the same voltage rating. The additional highly n doped buffer layer can reduce the minority carrier injection and decrease minority its carrier lifetime, and consequently increase the switching speed. Meanwhile, the additional n-doped layer may increase the saturation collector-emitter voltage $V_{ce,sat}$, and increases the conduction loss.

The trench-gate with Field Stop (FS) technology (in Figure 2.6(c)) further improves the characteristics: much thinner chip and faster switching speed. It is worth noting that all studies (simulations and tests) are based on the trench-gate FS IGBTs in this thesis.

IGBT operation modes can be illustrated by a schematic of a family of collector current versus voltage (I-V) curves in Figure 2.8, where the collector-emitter voltage (V_{ce}) is plotted on the horizontal axis, while the collector current (I_C) is on the vertical axis. When a negative voltage is applied to the IGBT collector, the PN junction formed by p+ substrate and n drift region is reverse biased. The maximum reverse-blocking (BV_R) and forward-blocking (BV_F) voltage capability are determined by the main PNP BJT's open base breakdown voltage. With sufficiently large gate voltage to ensure operation of the MOSFET region in its linear mode, the IGBT will work in on-state and behave as a P-i-N diode, as shown in Figure 2.8. With the gate bias above the threshold

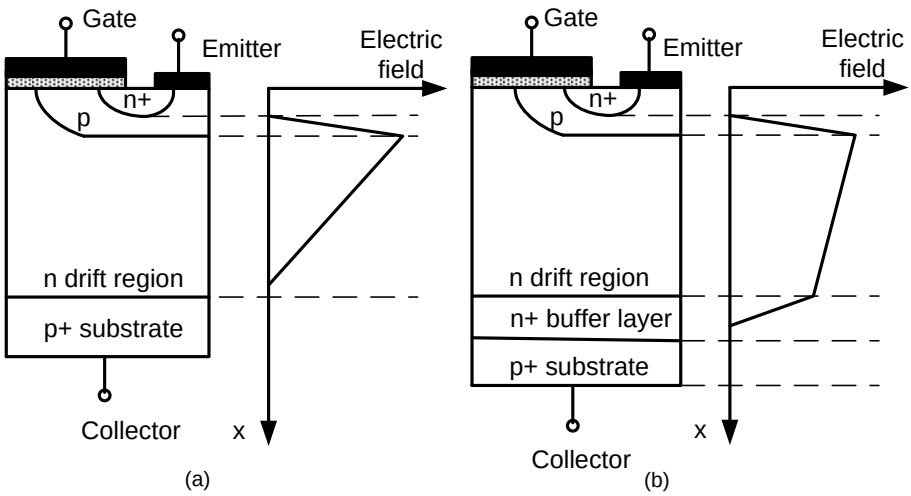

Figure 2.7: *The planer gate NPT and PT IGBT structures and corresponding electric fields: (a) planer gate NPT IGBT and electric field; (b) planer gate PT IGBT and electric field.*

voltage, the IGBT exhibits an active region with the collector current saturated at a specific value determined by the applied gate voltage, as illustrated by a family of curves in Figure 2.8.

2.3.2 IGBT Catastrophic Failures

As generally discussed in Section 2.1, the power semiconductors catastrophic failure can be classified into cosmic rays induced burnout, instabilities and severe overstress.

Cosmic rays induced failure

Cosmic rays induced failure has been discussed in detail in Section 2.2.2 for the power diode.

Instabilities

Instabilities of IGBT can be classified as Unclamped Inductive Switching (UIS) instabilities, overload-triggered instabilities, dynamic avalanche at turn-off, as well as oscillations during commutations.

UIS instabilities.

UIS condition means that the IGBT is turned off under inductive load without voltage clamp. In this case, the off-state voltage is limited only by the avalanche breakdown and the device withstands this very hard condition for several microseconds. UIS rarely happens during power converter normal operations, as it is usually caused by a sud-

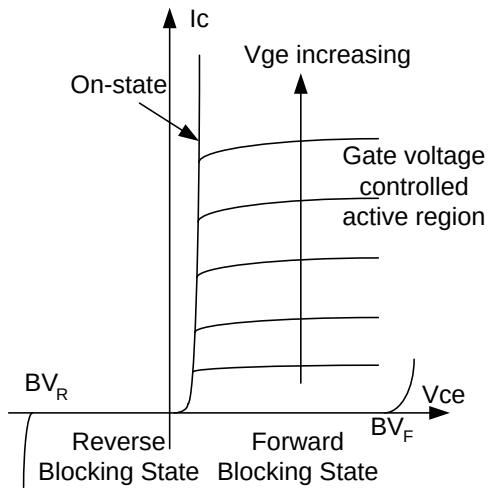

Figure 2.8: *IGBT collector current versus voltage (I-V) curves.*

den turn-off during overload or short circuit, as well as similar conditions. Because the switched current is very high in these cases, the *di/dt* gradient in the stray inductances can lead to high voltage.

Even the state-of-art trench-gate field-stop IGBTs are prone to UIS instabilities [40]. An experimental study from Toyota has identified the non-uniform current distribution on the chip back side as a root cause of instability during UIS [41].

Oscillations.

Gate-emitter voltage high frequency oscillations have been experimentally observed under short circuit conditions, especially the instability can be dangerous at the high voltage together with high temperature operations [42]. The basic mechanism originates from the increase in the PNP transistor's current gain (see Figure 2.5(b)) depending both on the temperature and the collector voltage. If this gain reaches a given threshold, because of holes accumulating under the gate oxide, a negative equivalent capacitance appears at the gate lead. The interaction between this capacitance and the external circuit may cause the formation of stable oscillations involving the gate voltage. In some cases the amplitude of these oscillations can become as large as to destroy the gate oxide. A recent study on the latest-generation IGBTs shows that it is still a critical issue [43].

Severe overstress

High voltage breakdown.

High voltage spikes induced by high falling rate of collector current (I_C) and stray

inductance can destroy IGBT during turn off, especially under repetitive stresses [44]. Due to the high turn off voltage spike, the electric field can reach the critical field and break down one or few IGBT cells first, and lead to high leakage current as well as high local temperature. Subsequently, the heat-flux radially diffuses from the over-heated region to the neighboring cells. Collector-emitter voltage (V_{CE}) collapses after the voltage spike, and then I_C rises again. Also, the gate terminal may fail, which results in gate voltage (V_{GE}) rising up.

High value of V_{CE} and V_{GE} can also lead to short circuit during turn-on. An abrupt destruction and peak current happens after several microseconds during turn on. The hole current caused by the avalanche generation concentrates on a certain point (usually high doped $p+$ region). The destruction point is always located at the edge of the active area close to device's peripheral region [45]. Therefore, it is critical to clamp V_{GE} and V_{CE} during the switching transients.

Static and dynamic latch up.

Latch up is a condition where the collector current can no longer be controlled by the gate voltage [46]. With respect to Figure 2.6(b), the latch up happens when the parasitic NPN transistor is turned on, and works together with the main PNP transistor as thyristor, and then the gate loses control of I_C. IGBT latch up can be divided into two types, a static and a dynamic latch up. The static latch up happens at high collector currents, which turn on the parasitic NPN transistor by increasing the voltage drop across the parasitic resistance R_S. The dynamic latch up happens during switching transients, usually during turn off, when the parasitic NPN transistor biased by the displacement current through junction capacitance C_{cb} between the deep $P+$ region and the $N-$base region. There are two distinct conditions that may lead to a dynamic latch up. One is when the gate voltage drops very fast and induces excessive displacement current through the gate oxide that flows through the parasitic resistance. The other one is when the off state collector-emitter voltage is quite high and induces excessive charging currents within the IGBT during the switching transient, which will flow through the parasitic resistance. Both conditions may trigger the parasitic NPN transistor and eventually lead to a latch up. It should be noticed that the collector current leading to a dynamic latch up is lower than that of a static latch up.

When a latch up happens, the IGBT will be almost inevitably damaged due to the loss of gate control. Therefore, several methods are proposed to predict latch up, especially based on the collector emitter on voltage $V_{CE(on)}$ and turn off time [45] [47]. It is worth to mention that the latest generation IGBTs with a trench-gate structure and a heavily doped $P-$base region under $N-$emitter region have been proved to behave good latch up immunity [48], and the latch up is not a common failure in the latest devices anymore.

Second breakdown.

Second breakdown is a kind of local thermal breakdown for transistors due to high current stress, which can also happen to IGBTs during on state and turn off.

The failure mechanism of second breakdown is as follows: with the increase of current, the collector base junction space charge density increases, and the breakdown voltage decreases, resulting in a further increase in the current density. This process continues until the area of the high current density region reduces down to the minimum area of a stable current filament. Then, the filament temperature increases rapidly due to self-heating and a rapid collapse in the voltage across the IGBT occurs. How to improve IGBT ruggedness at high current density and prevent second breakdown is still an interesting research topic [49].

Energy shocks.

During short circuit at the on state, failure may happen due to high power dissipation. The high power dissipation within a short time is defined as energy shock. The high short circuit current will result in energy shock and high temperature. However, IGBT will not immediately fail even if the junction temperature exceeds the rated temperature. Until reaching the intrinsic temperature, further rise in junction temperature would lead to exponential increase in the carrier concentration and thermal runaway. With further increase of temperature, the silicon die may become fatally damaged and the contact metal may also migrate into the junctions.

Even the short circuit current is successfully turned off, short circuit failure could still happen after several microseconds, which is called delayed failure in [48]. It is further verified by experiments and numerical simulation that large leakage current leads to the thermal runaway [50]. A "critical energy (E_C)"is proposed to explain the mechanisms of catastrophic failure and wear out failure under repetitive short circuit operations. When short circuit energy is below E_C, the IGBT may survive for more than 10^4 times repetitive short circuit operations before failing. However, when short circuit energy is far beyond E_C, the IGBT may fail after first short circuit due to thermal runaway. A further experimental investigation show that IGBT can turn off successfully after short circuit but fails after several microseconds when the short circuit energy is lightly higher than E_C. It is still challenging to determine the exact value of E_C, even though many experiments and numerical simulations have been done in the prior-art research [51].

A recent research also demonstrates this failure mechanism in trench gate field-stop structure IGBT by comprehensive experiments [52]. Because the trench-gate field-stop IGBT has a smaller heat capacity, it is preferable to improve the thermal performance. A state-of-the-art method is to use a thicker front side metallization, made of copper instead of aluminum, and a newly developed diffusion soldering process to attach the direct bonded copper (DBC) substrates. It can increase the short circuit capability, for instance E_C by 80% according to simulation studies [53] [54].

A summary of IGBT overstress failure mechanisms is presented in Table 2.1. As discussed before, short circuit currents inevitably introduce high energy and temperature to IGBT chips, and the thermal behavior is closely related to the high junction temperature and local hot spots. Therefore it is important to precisely study the electro-thermal behavior of IGBTs under short circuits in order to provide protection guidelines and to

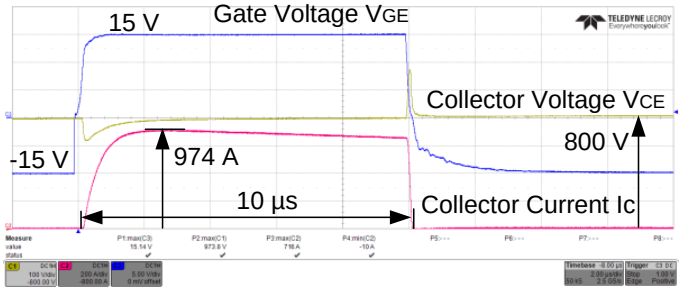

Figure 2.9: *Experimental waveforms of short circuit Type I test of a 1.7 kV / 150 A IGBT power module performed at 800 V of collector voltage. Time scale: 2 µs/div; gate voltage: 5 V/div; collector voltage: 200 V/div; collector current: 200 A/div.*

improve the thermal management.

2.4 IGBT Short Circuit

IGBT short circuit working conditions can be caused by internal mechanisms as well as the external circuit, and the IGBT is working in the gate voltage controlled active region, suffered both high voltage and saturated current. The short circuit operations can be classified as Type I and Type II according to the electrical behavior.

2.4.1 IGBT Short Circuit Operations

Short circuit Type I happens at the turn on of the IGBT. Before turn on, the gate voltage is negative and the collector-emitter voltage V_{CE} is high. Immediately after turn-on into short circuit, the collector current increases to several times of the rated current, which is the value of the saturated current at V_{GE}=15V. IGBT should be turned-off within short duration (typically less than 10 μs claimed by manufacturers). An experimental example is given in Figure 2.9.

Short circuit Type II happens during the IGBT conducting mode. The main difference with short circuit Type I is the beginning of the desaturation phase, which may increase the V_{GE} and a high short-circuit current peak [55]. After the desaturation phase, short-circuit current will drop to its static value I_{SC}, and the subsequent behavior is the same as short circuit Type I. Short circuit Type II is harsher in converter operations due to the potential oscillations and collector overvoltage. Because short circuit Type I performance is more closely related to the device's own characteristics, all simulations and experiments in this project focus on short circuit Type I.

Table 2.1: *Summary of IGBT severe overstress failure mechanisms*

Failure Mechanisms	**Failure Behavior**	**Failure Location**	**Thermal Behavior**
High voltage breakdown	During turn-off: V_{CE} collapses and I_C rises after voltage spike	At the edge of active area	Overheating on few peripheral cells at first, and then spreads to the whole chip
	During turn-on: peak high I_C results in destruction		
Latch-up	Static latch-up during on-state: high I_C leading to loss of gate control	Active area	Overheating on a stable subset of cells of the device
	Dynamic latch-up during transients: high dv/dt leading to loss of gate control		
Second breakdown	Local thermal breakdown due to high currents	Emitter regions	Very high local temperature spots
Energy shocks	$E > E_C$ (critical energy): thermal runaway after successfully turned-off	Emitter regions	Very high local temperature spots
	$E < E_C$: degradation of die metallization	Al metallization layer, bond wires lift off	Local overheating of Al metallization layer after 10^4 cycles

2.4.2 Challenges Induced by Short Circuits

Short circuit is a critical working condition for an IGBT, the high voltage and high current will induce high energy shock within several μs. The high temperature, high di/dt will lead to instabilities - oscillations for both Type I and Type II short circuits.

Type II short circuit oscillations have been investigated in the literatures. Gate voltage oscillations have been experimentally observed during on-state short circuits for both IGBTs housed in power modules and in IGBT press-packs [56] [57].

Type I short circuit oscillations are rarely discussed, especially for high power modules. Figure 2.10 displays an example of oscillations from a commercial 1.7 kV/1 kA IGBT power module under Type I short circuit. The duration shown in Figure 2.10 is far below the demands of many IGBT applications engineers, which is around 10 μs.

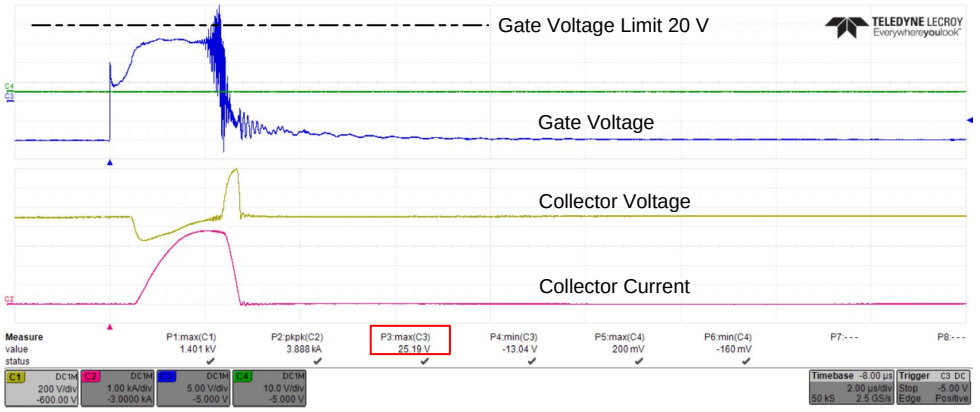

Figure 2.10: *Evidence of oscillations occurring during a short circuit test of a 1.7 kV / 1 kA IGBT power module performed at 900 V of collector voltage. Time scale: 2 µs/div; gate voltage: 5 V/div; collector voltage: 200 V/div; collector current: 1 kA/div. The gate peak voltage was 25.19 V, whereas the absolute maximum rating for this device is 20 V.*

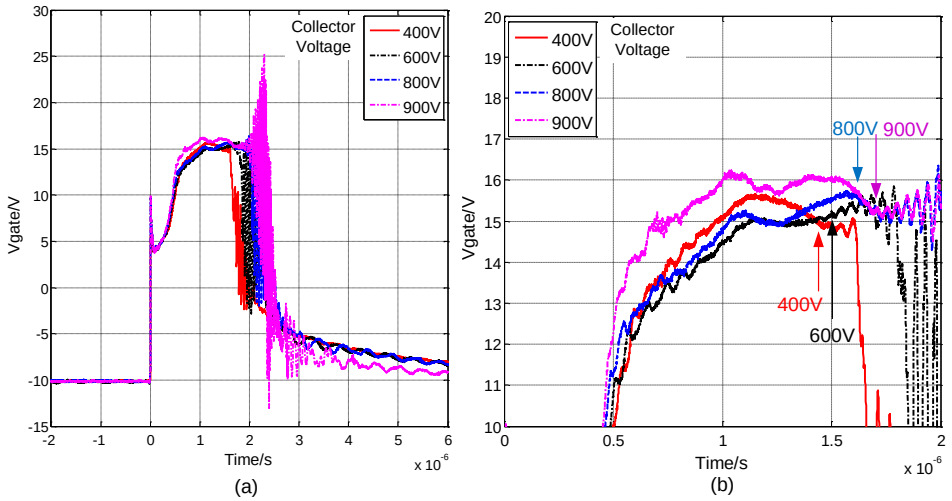

Figure 2.11: *Study of the oscillations' occurrence on the gate voltage at different collector-emitter voltages: (a) gate voltage waveforms obtained at increasing collector voltages from 400 V to 900 V, (b) details of the same waveforms before the IGBT turn-off from t=0 to t=2 µs.*

To further investigate the dependence of the above phenomenon on the operating conditions, several more experiments have been performed at different collector voltages. Figure 2.11(a) shows the gate waveforms obtained at increasing voltages from 400 V to 900 V. Figure 2.11(b) depicts the details of the same waveforms from t=0 to t=2 μs. The oscillation beginnings are indicated by arrows. Evidently, it appears from Figure 2.11(b) that the oscillations commence after a time delay that increases with the applied voltage.

Due to the large energy generated during a short circuit, the chip junction temperature cannot be assumed to remain constant. In fact, a large temperature peak in the order of hundreds of degree can occur. This temperature dependence aids the interpretation of the oscillations occurrence. Referring to Figure 2.11, applied voltage influences the delay before oscillations commence. Short circuit at higher collector voltages will consequently lead to higher temperature. Therefore, an accurate evaluation of junction temperature is highly required to further study this phenomenon during short circuits.

2.5 Summary

This chapter summarizes the common failure modes of modern power semiconductor devices. It further summarizes some typical catastrophic failure mechanisms of power diodes and IGBTs, and the high junction temperature is an important indicator of failure. Afterwards, it gives special attentions to the IGBT short circuit mechanism and corresponding reliability issues. Instabilities during short circuit also suggests that junction temperature estimation is very important, which will be studied in detail in next two chapters.

Chapter 3

A Physics-based Electro-thermal Modeling Method of IGBT Modules under Abnormal Conditions

This chapter proposes a physics-based PSpice-Icepak co-simulation method. It combines a physics-based, device-level, distributed PSpice model with a thermal Finite-Element Method (FEM) simulation, gaining the possibility to take into account the electro-thermal coupling effects and uneven distribution of electro-thermal stresses among chips. Case studies on one section of the commercial 1.7 kV/ 1 kA IGBT power modules are given for both a new device and a degraded device.

3.1 Principles of Electro-thermal Analysis

In Chapter 2, it is stated that the junction temperature (Tj) is one of the most critical parameters for IGBT catastrophic failures during the abnormal conditions. Therefore, it is desirable to accurately estimate the junction temperature as well as simulate hot spots in order to determine the IGBT modules robustness margins and prevent the potential failures with high confidence levels. A precise electro-thermal modeling method is demanded for such an analysis.

3.1.1 Fundamentals of Heat Transfer and Thermal Analysis

It is important to understand the basic mechanisms of heat transfer and to consider the fundamental equations for evaluating the heat transfer. There are three modes of heat transfer: conduction, convection, and radiation [58]. All heat-transfer processes involve one or more of these modes.

Heat transfer by conduction is accomplished by two mechanisms: the first is the molecular interaction in which the greater motion of a molecule at a higher energy level (temperature) imparts energy to adjacent molecules at lower energy levels. The second mechanism is the heat transfer by free electrons, which are significant primarily in pure-metallic solids. The heat conduction is primarily a molecular phenomenon, which can be described by the Fourier equation:

$$\frac{q_{condx}}{A} = -k\frac{dT}{dx} \tag{3.1}$$

where q_{condx} is the heat-transfer rate in the x direction, the unit is in Watts; A is the area normal to the direction of heat flow, in m^2; dT/dx is the temperature gradient in the x direction, in K/m; and k is defined as the thermal conductivity, in $(W/m-K)$. The negative sign in equation (3.1) indicates that heat flow is in the direction of a negative temperature gradient. It is worth mentioning that the thermal conductivity is a property of a conducting medium and is primarily a function of temperature. Failing to consider this temperature effects can lead to improper results in thermal analysis, which will be further discussed in the next sections. The ratio q_{condx}/A, in W/m^2, is referred to the heat flux in the x direction. A more general relation for the heat flux is equation (3.2):

$$\frac{\vec{q}_{cond}}{A} = -k\nabla T \tag{3.2}$$

which indicates the heat flux is proportional to the temperature gradient. Equation (3.2) is often referred to as Fourier's first law of heat conduction. Consider the case depicted in Figure 3.1, the steady state conduction through a plane wall with its surfaces held at constant temperatures T_1 and T_2. By solving the Fourier rate equation for the x direction in (3.1), the equation below for a q_{condx} subject to the boundary conditions $T = T_1$ at x= 0 and $T = T_2$ at x=L:

$$\frac{q_{condx}}{A}\int_0^L dx = -k\int_{T_1}^{T_2} dT = k\int_{T_2}^{T_1} dT \tag{3.3}$$

or

$$q_{condx} = \frac{kA}{L}(T_1 - T_2) \tag{3.4}$$

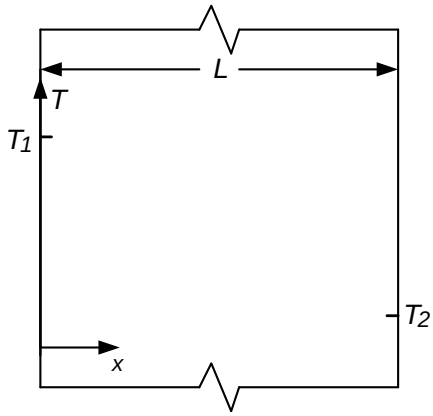

Figure 3.1: *Example of a steady-state conduction of heat through a planar wall.*

Heat transfer due to convection involves the energy exchange between a surface and an adjacent fluid. The convective heat transfer can be expressed by Newton's law of cooling:

$$\frac{q_{conv}}{A} = h\Delta T \tag{3.5}$$

where q_{conv} is the rate of convective heat transfer, in W; A is the area normal to direction of heat flow, in m^2; ΔT is the temperature difference between surface and fluid, in K; and h is the convective heat transfer coefficient, in $W/m^2{\cdot}K$. The coefficient h is, in general, a function of system geometry, fluid and flow properties, and the magnitude of ΔT.

The radiant heat transfer between surfaces requires no medium for the propagation, which differs from conduction and convection. The heat transfer by radiation reaches maximum, when the two surfaces that are exchanging energy are separated by a perfect vacuum. The rate of energy emission from a perfect radiator or a black body is given by:

$$\frac{q_{rad}}{A} = \sigma T^4 \tag{3.6}$$

where q_{rad} is the rate of radiant energy emission, in W; A is the area of the emitting surface, in m^2; T is the absolute temperature, in K; and σ is the Stefan-Boltzmann constant, which is equal to $5.676 \times 10^{-8}\ W/m^2{\cdot}K^4$. Equation (3.6) is most often referred to as the Stefan-Boltzmann law of thermal radiation.

In real applications, heat transfer is normally accomplished by a combination of the aforementioned mechanisms. It would be beneficial to obtain a combined way of calculating heat transfer rates when several transfer modes were involved, for instance both conduction and convection. Equation (3.4) is very similar to the Newton rate

Table 3.1: *Correspondence between electrical and thermal parameters.*

Electrical Parameters	**Thermal Parameters**
Voltage, U (V)	Temperature difference, ΔT (K)
Current, I (A)	Heat flow, P (W)
Resistance, R (V/A)	Thermal resistance, R_{th} (K/W)
Capacitance, C (As/V)	Thermal capacitance, C_{th} (Ws/K)

equation (3.5). This similarity can be utilized in a problem in which both types of heat transfer are involved. What's more, the thermal impedance theory can be generalized accordingly. The analogous quantities in the expressions for heat flow and electrical current are apparent, as shown in Table 3.1. The thermal resistance Rth between two positions is defined as the temperature difference divided by the heat flow:

$$R_{th} = \frac{\Delta T}{P} \tag{3.7}$$

Another common way of conducting thermal analysis is to solve the basic heat transfer differential equations by means of the numerous methods. In a situation where there is no fluid motion and all heat transfer is by conduction, the general differential equation for heat transfer is:

$$\rho c_p \frac{\partial T}{\partial t} = \nabla \cdot \left[\vec{k} \nabla T(\vec{r}, t) \right] + \dot{q} \tag{3.8}$$

where r is the location, t is time, ρ is the density, c_p is the heat capacity at constant pressure, $\dot{q}$ represents the heat generation effects.

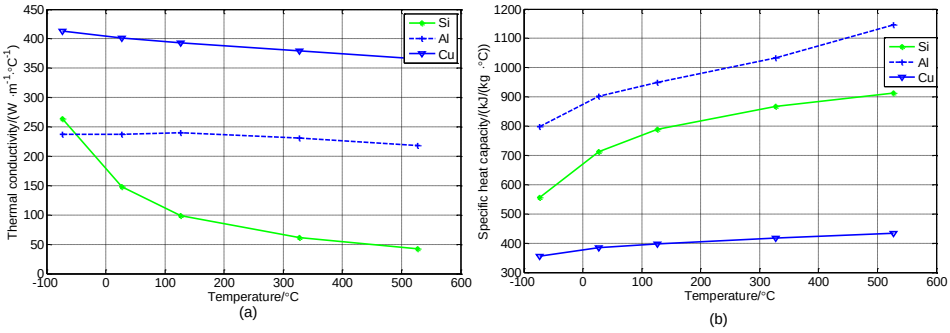

Figure 3.2: *Temperature effects on the thermal properties of Si, Al, and Cu: (a) thermal conductivity; (b) specific heat capacity.*

The first term of equation (3.8) is the transient properties of the temperature. The first term on the right in (3.8) is the steady state heat conduction. The final term on the right is the change in stored internal energy. Equation (3.8) can be solved by a finite element approach with the help of the commercial Finite Element Methods software, for instance ANSYS/Icepak [59] or COMSOLMultiphysics [60].

Table 3.2: *Common materials thermal properties at different temperatures.*

Temperature		25 °C	75 °C	125 °C	225 °C	325 °C
Si	Thermal Conductivity (W/m-K)	148	119	98.9	76.2	61.9
	Heat Capacity (J/kg-K)	705	757.7	788.3	830.7	859.9
Al	Thermal Conductivity (W/m-K)	237	240	240	236	231
	Heat Capacity (J/kg-K)	897	930.6	955.5	994.8	1034
Cu	Thermal Conductivity (W/m-K)	401	396	393	386	379
	Heat Capacity (J/kg-K)	385	392.6	398.6	407.7	416.7

Equation (3.2) shows that the heat transfer by conduction is related to the thermal conductivity, which in a first approximation can be considered as independent of temperature [61] [62] [63]. The prevalent materials for IGBT modules are Silicon (Si), Aluminium (Al) and Copper (Cu). The thermal conductivity, heat capacity and density information of these typical materials used in the power module at different temperature is listed in Table 3.2 [58], [64]. It can be seen that for the range of temperatures considered in this work (from 25 °C to several hundreds of °C), the constant approximation is not sufficiently accurate. The temperature effects on the thermal parameters of Si, Al, and Cu are further plotted in Figure 3.2. According to Table 3.2 and Figure 3.2, it can be seen that the thermal conductivity of silicon decreases strongly with an increasing temperature; the exact opposite is the case with the pressure specific heat capacity. The silicon thermal conductivity around 250 °C is only half of the value around 25 °C. Based on this, it is clear that the power module thermal behavior depends directly on the local temperature [65]. This point is very critical for overloads and short-circuit analysis, where the chip temperature rises dramatically (several hundreds of °C), even if for limited time duration (in the range of several milliseconds). Therefore, this nonlinear temperature behavior will also be included in the FEM model to improve the simulation accuracy.

3.1.2 IGBT Electrical Model

Over the past decades, plenty of research efforts have been devoted to develop accurate and reliable models for IGBTs. Based on the different modeling method, the IGBT models can be classified into about three kinds: Finite-Element Modeling (FEM) models, behavior models and circuit models.

The FEM models are developed based on the finite element methods, or partially coupled FEM methods [66], [67]. They are normally used to analyze the cell-level electro-thermal characteristics of the power devices [68]. It is also worth noting that the physical cell-based (i.e., in the scale of few square microns) FEM simulation can hardly predict temperature distribution among several cells, which is critical for studying the thermal performance of high power IGBT modules.

Another method is to derive the model parameters by fitting the model characteristic waves with the experimental results [69], [70]. This kind of modeling methods focuses more on the behavior of the IGBTs, like the switching procedure, the output characteristics and the transfer characteristics. For this reason, they are often called "behavioral models".

The circuit models here are the models developed based on the IGBT equivalent circuits, which model the physics characteristics of the IGBT at different degrees [71] [72]. The models are usually provided with the complete parameters' identification procedure.

In this study, a physics-based IGBT lumped-charge model in PSpice is adopted, which has shown accurate results, high modularity and also fast simulating speed [73]. Experimental validations also evidence that it is suitable to simulate normal as well as abnormal conditions.

3.1.3 State-of-art in IGBT Electro-thermal Analysis

So far, electro-thermal co-simulations are prevailed in integrated circuit simulations and optimizations, which are hard to extend to the power semiconductor study because the corresponding physics-based electrical models are absent [74], [75]. Some researchers attempted to extend widely-used electrical simulation tools (e.g., Spice, Saber) to electro-thermal simulations by introducing lumped thermal impedance. However, this method cannot provide accurate junction temperature as well as temperature distribution, because there are only a few thousands intrinsic nodes in such tools, which are not enough to guarantee the accuracy [76] [61] [77] [78]. Similarly, a compact electrical model can be integrated with a distributed 3D mathematical description of the thermal phenomena [79], [80], which can reduce the computing time but also the accuracy. FEM software can have a dramatic reduction in simulation speed and accuracy when a multi-physics approach is adopted. For instance, thermal simulator Icepak [59] connected with circuit-level simulator Simplorer [81] in ANSYS leads to a heavy and slow process (seconds per simulation point). The IGBT model in Simplorer is based on the electrical behavior, which may not be suitable for abnormal operation studies. Moreover, this intrinsically single-cell approximation method unavoidably loses plenty of information, e.g., uneven fast junction temperature variation and unstable thermal dynamics inside IGBT chips, which strongly limit the prediction of imbalances among the cells of the real device. Another solution - physical cell-level (i.e., in the scale of few square mi-

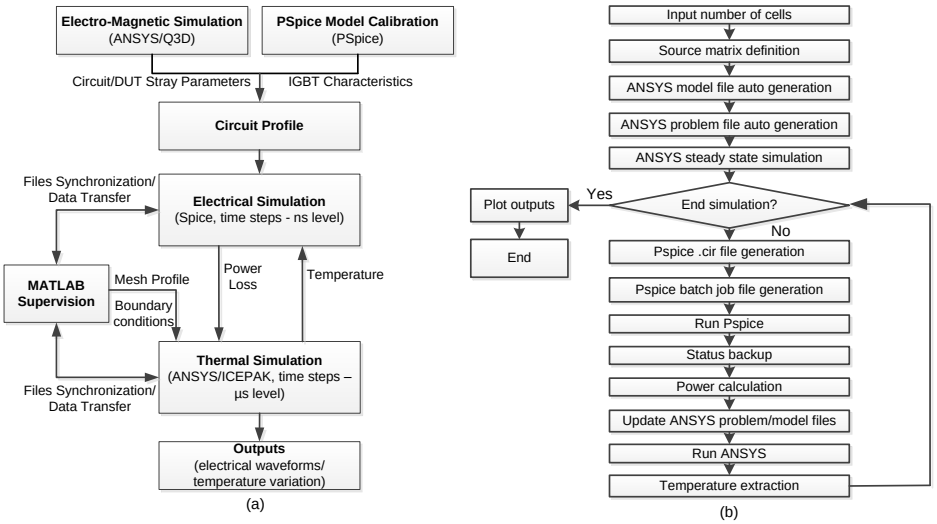

Figure 3.3: *Principle of the proposed electro-thermal modeling method: (a) the structure; (b) MATLAB script flow chat.*

crons) FEM simulation, like TCAD, can hardly predict temperature distribution among several cells [68], which is critical for studying the short-circuit behavior.

3.2 PSpice-Icepak Co-simulation Description

This study proposes a novel perspective for electro-thermal co-simulation, which connects a physics-based, device-level, distributed electrical simulation tool with a thermal FEM simulation in order to obtain high accuracy on both the electrical side and the thermal side. It can also gain another advantage - independent time steps can be adopted for the electrical and thermal parts, thus gaining improved calculation efficiency. A physics-based IGBT model in PSpice is adopted, since it has shown accurate results, high modularity ability and also fast simulating speed, which is suitable to simulate normal as well as abnormal conditions [73].

3.2.1 Basic Principle

The proposed method includes three major parts: PSpice simulation based on a physics-based, device-level IGBT PSpice model, thermal analysis in ANSYS/Icepak, and a monitoring program in MATLAB. The MATLAB script is implemented to prepare configuration files and then coordinate data transfer at each thermal simulation step between

the above two packages. The co-simulation structure and process is illustrated in Figure 3.3(a). The operation is divided into preparation state and simulation state.

At the preparation state, the IGBT model is calibrated based on the datasheet, and the stray parameters of the devices and circuit is set, as well as the electrical simulation profile is defined, for instance the simulation type (e.g., short circuits or overloads), duration, and external voltage. Meanwhile, the device geometry is built and meshed in FEM software and the initial and boundary conditions are defined. The MATLAB script can automatically divide the chips of the Device Under Test (DUT) in an arbitrary number of virtual cells. The only condition required is that it should be rectangle-shaped. In the study case for one IGBT chip, 4-by-4 arrays of cells have been adopted (see Fig. 3.3(a)), which include power sources placed in the body of the IGBT chip. The MATLAB script also prepares the temperature monitoring points for each IGBT cell, as well as generates one PSpice sub-circuit from a circuit template file, which includes the parameter identified for the considered device.

At the simulation state, the MATLAB script synchronizes the PSpice and Icepak simulations and coordinates the data sharing between them. Starting from the definitions of the initial and the boundary conditions, the electrical problem is solved in PSpice with the time resolution of nanoseconds. The PSpice simulation lasts a thermal time step (typically in the range of microseconds) and it is paused. MATLAB script transfers the dissipated power losses to the thermal simulation – the corresponding power loss function files in Icepak are updated accordingly. Subsequently the thermal analysis is performed for a thermal time step by means of the differential equations in ANSYS/Icepak. The iterative solution of the thermal problem lasts until the convergence criterion is satisfied. At the end of the thermal analysis, a new temperature distribution in the structure is computed and transferred to PSpice, leading to a continuing electrical simulation in order to evaluate the new current and power loss distribution. This process is illustrated in Figure 3.3(b), which continues until the end of the simulation. A MATLAB script sample is given in the Appendix.

3.2.2 PSpice File Format

Before the co-simulation, the user defines the desired simulation profile. Some typical simulation profiles are: normal operation, overload and short circuit. Then, the IGBT model is automatically generated as a PSpice circuit containing an arbitrary number of IGBT cells with an emitter resistance network, as shown in Figure 3.4(a), which are used to model the bond wires fatigue and Al layer reconstruction, and also to predict the consequent thermal effects.

A physics-based lumped-charge model has been instantiated for each cell, which has demonstrated an improved accuracy and comparable simulation speed for high voltage IGBTs compared to the widely used classical PSpice model. The principle is subdividing the semiconductor into a few regions characterized by constant doping and/or

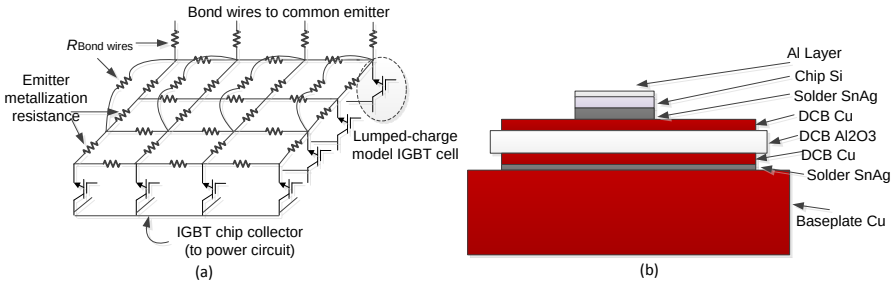

Figure 3.4: *Simulation models of IGBT: (a) electrical model with emitter resistance network (4 by 4 cells); (b) cross-section of the multilayers in a typical IGBT power module.*

carrier lifetime, and the behaviour of each region is described by means of a few lumped charges placed in proper aggregation points. A few parameters are required to identify the model, which can be obtained from the datasheets and manufacturers: chip area, stray resistance, stray inductance, and gate capacitances. With all the aforementioned information defined, a PSpice circuit file is generated by the MATLAB supervision script based on the template file. A PSpice template file is given in the Appendix.

3.2.3 ANSYS/Icepak Program

A detailed Icepak geometry model is necessary for the thermal simulations. All geometry and material information are defined in the Icepak "model" file. It also includes the power loss information before simulations, which will be updated by the PSpice electrical simulation during the co-simulation process. All thermal simulation setting information is included in the Icepak "problem" file. It defines the thermal simulation step and ending time of the simulation. The monitoring points are set for each IGBT cell, which can record the temperature information after each thermal simulation step. The temperature map will be fed back later to the next electrical simulation in PSpice. The locations of these points are also included in the "problem" file. After the "model" and "problem" files have been defined by the MATLAB supervision script, the co-simulation starts.

Two aspects should be carefully considered to guarantee the FEM simulation accuracy: (1) a detailed 3-dimensional geometrical model with fine mesh; (2) precise information of the material properties, especially the temperature-dependent effects.

First of all, the geometry of the DUT is measured by means of an open power module without the plastic frame and silicone gel. The layers' cross-section information is obtained by a micro-sectioning approach combined with optical microscopy. A cross-section structure and the materials used of a typical IGBT power module are shown

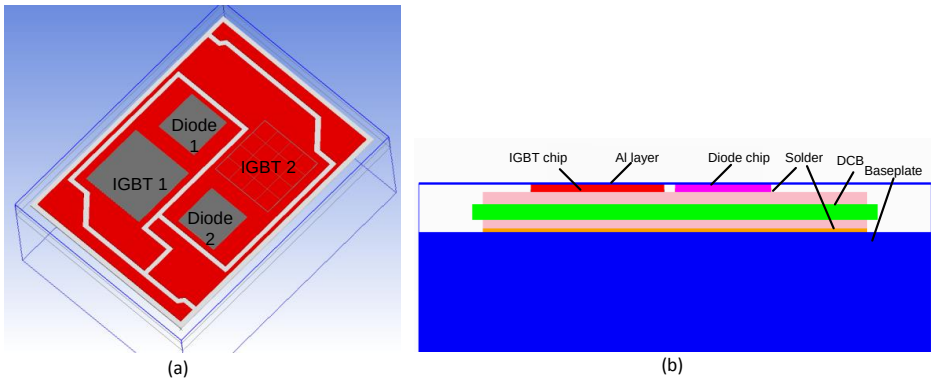

Figure 3.5: *Thermal model of one section of IGBT power module constructed in Icepak: (a) 3D view of the geometry, (b) details of the cross section on the vertical plane.*

in Figure 3.4(b). From top to bottom, a typical IGBT module contains: Al layer, Si chip, solder for chip, Direct Copper Bonded (DCB) layers, solder for baseplate, and Copper (Cu) baseplate. The IGBT chip is 12.6 mm×12.6 mm square shape, and is based on a trench-gate technology. The trench-gate structure is prevailed in modern IGBT devices, because it can reduce on-state voltage drop comparing with a planar-gate IGBT under the same blocking voltage capability, especially for devices with high switching speed. The gate region is formed after the diffusion of the P-base and N+ emitter regions. The gate oxide is formed on the surface of the trench followed by the deposition of poly-silicon as the gate electrode. The poly-silicon is planarized to recess the gate electrode slightly below the silicon surface. On the top of emitter, there is a very thin Al metallization layer (several μm). Therefore, three layers are modeled for the chip: Al metallization layer, gate layer and body layer, where individual thermal parameters are defined independently. The power source is located in the IGBT body layer. Accordingly, a higher meshing resolution is applied to the active region of the chip, where both the electrical and the thermal field gradients are the highest. 543,000 nodes are defined in the Icepak model. The one IGBT section's geometry is illustrated in Figure 3.5(a), while the cross-section structure in Icepak is shown in Figure 3.5(b).

3.3 Case Studies of One IGBT Section

In order to illustrate the proposed PSpice-Icepak co-simulation method, a case study of 1.7 kV/1 kA commercial IGBT module is given in this section. The main specifications of the IGBT module are shown in Table 3.3. There are six sections in parallel inside

Table 3.3: *Main specifications of the IGBT module under investigations.*

Specifications	**Value**
Collector-emitter voltage, V_{CES}	1.7 kV
Continuous DC collector current, I_{Cnom}	1 kA
Total power dissipation	6.25 kW
Temperature under switching conditions	-40 °C $\sim$ 150 °C
Operation Temperature, T_{vjop}	150 °C
Rated short-circuit current, I_{SC}	4 kA
Gate-emitter maximum voltage, V_{GES}	$\pm$20V
Gate threshold voltage, V_{GEth}	5.8 V
Gate charge, Q_G	10 μC
Internal gate resistance, R_{Gint}	1.5 Ω
Number of parallel sections	6
Thermal resistance of junction to case, R_{thJC}	24 K/kW

the IGBT module. In this chapter, only one IGBT section is studied in order to focus on the chip level electro-thermal behavior. Each section includes two IGBT chips and two freewheeling diode chips, which are configured as a half-bridge. The IGBT chip is based on the field-stop trenched-gate technology.

3.3.1 Case Study I: Short circuit of a New IGBT

One of the most critical abnormal working conditions for IGBTs is short circuit, where both high voltage and high current are applied to the device concurrently. Before the co-simulation, a simulation profile is selected: a gate-emitter voltage V_{GE} pulse with the amplitude of 15 V, pulse length of 10 μs, DC voltage of 700 V. Then, the IGBT model is automatically generated as a PSpice circuit containing an arbitrary number of IGBT cells with an emitter resistance network, as shown in Figure 3.4(a). In the electrical model, the studied IGBT chip is divided into 4 by 4 cells. According to the information from the manufacturer, the IGBT module's stray inductance is 10 nH, its gate capacitance is 81 nF, while the IGBT chip is physically 12.6 mm by 12.6 mm square size. The corresponding IGBT lumped charge model can be obtained according to the method discussed in [5]. With all the aforementioned information defined, a PSpice circuit file is generated by the MATLAB supervision script before the co-simulation starts. The geometry information of one section in the Icepak is shown in Figure 3.5(a), and the cross section of the Icepak model is shown in Figure 3.5(b). The power source is located in the IGBT body layer. 543,000 nodes are defined in Icepak model. The thermal conductivity and heat capacity information of the materials used in the simulations are listed in Table 3.2. For the tens-of-μs-level short circuit simulations, the boundary

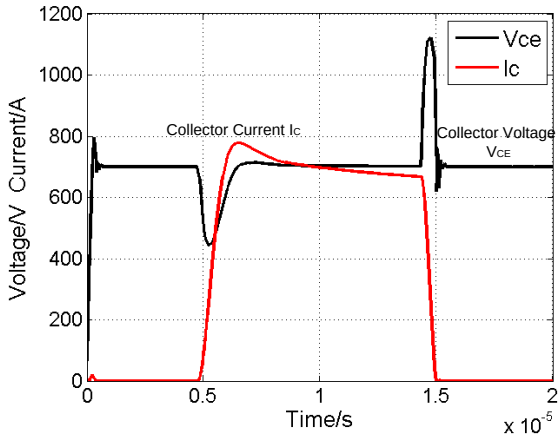

Figure 3.6: *Simulated collector current/voltage waveforms of the IGBT chip under 700 V/10 μs short circuit.*

conditions could be settings as: neglecting the thermal effect of the heat sink, the convective heat transfer at chip surface.

When a short circuit happens during the IGBT turn-on (at 5 μs), the collector current I_C rises rapidly until reaching the saturated current of 780 A. It is noted that the IGBT chip's rated current is only around 160 A. Due to the high current slope *di/dt* and the stray inductance, there is a voltage drop during the short-circuit turn-on, at the collector voltage waveform. The PSpice simulation results are plotted in Figure 3.6. The voltage overshoot during the short-circuit turn-off is also because of the high current slope *di/dt* and the stray inductance. According to the semiconductor physics, IGBT short circuit current decreases with the junction temperature rising because the transconductance is dropping with temperature [46], which is also evidenced in the simulations. The simulation waveforms will be further compared with the experiments under the same operating conditions in Chapter 5.

Four chip temperature maps obtained during short circuit are depicted in Figure 3.7. They are before short circuit (at 2 μs), during short circuit (at 10 μs and 14 μs), and after short circuit (at 18 μs), respectively. In the study case, temperature rises almost uniformly on the whole chip, and the periphery cells are only a bit colder than central ones. After the turn-off of short circuit, the temperature keeps rising due to the heat flow from the Si layer. IGBT chip's temperature rises to a temperature more than 150 °C at 18 μs due to the high energy shock in these conditions.

The "delay failure" modes in short circuits [3-27] can be explained by the heating effects, where IGBTs may fail at several μs to several tens of μs after successfully turned-off short circuits. One experimental observation of such a failure is given in Figure 3.8. The 1.7 kV/1 kA IGBT module has been tested under 800 V collector voltage

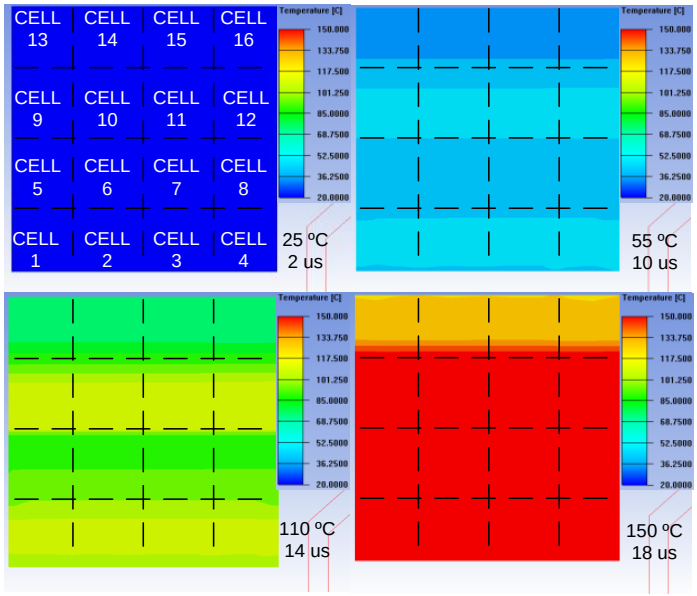

Figure 3.7: *IGBT power module chip temperature maps in Icepak during short-circuit at 2/10/14/18 µs (times and highest temperature at bottom right of each image) (temperature color bar – max 150 °C, min 20 °C).*

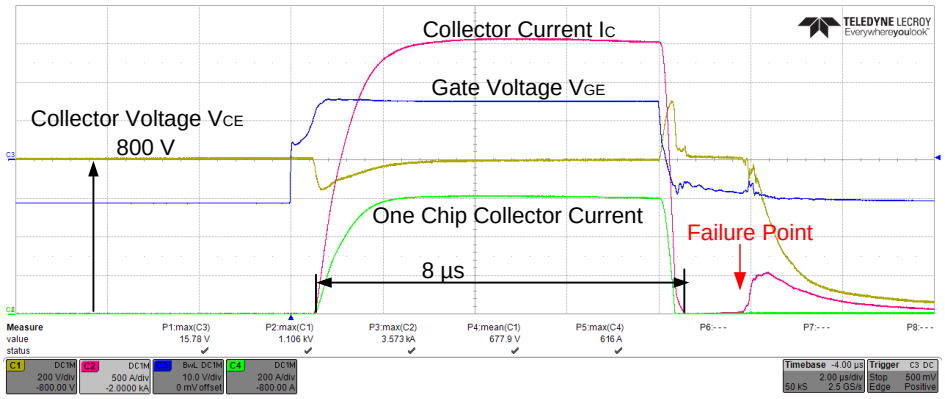

Figure 3.8: *Experimental waveforms of the "delay failure" for the 1.7 kV/1 kA IGBT module during a 800 V/10 µs short circuit: time scale 2 µs/div, collector voltage 200 V/div, collector current 500 kA/div, gate voltage 5 V/div, one chip collector current 200 A/div.*

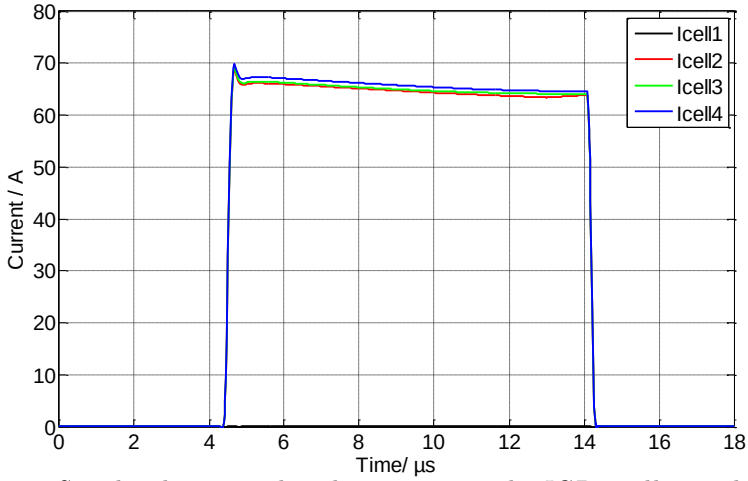

Figure 3.9: *Simulated current distribution among the IGBT cells 1-4 during short circuit (cell 1 current is almost zero due to the lifted bond wire).*

short circuits repetitively, and Figure 3.8 shows waveforms of the last test. The whole module's collector voltage, collector current, and gate voltage waveform, as well as one IGBT chip's collector current waveform are recorded in Figure 3.8. The test profile is gate voltage 15 V, collector voltage 800 V, short circuit duration 8 μs. The DUT successfully turned-off the short circuit current at 8 μs, however, it fails at around 2 μs after the short circuit ended. The failure point is marked with a red sign, where the collector voltage collapsed, and the collector current started increasing again. This failure can be explained by the relatively high junction temperature even after the short circuit, as shown in the simulations. It should be pointed out that the fault current is cut off thanks to the protections, which will be illustrated in details in Chapter 5. It is also worth noting that the failure does not happen for all the six parallel IGBT chips, because the collector current of one monitored IGBT chip is not increasing when failure happens (the green curve in Figure 3.8). This phenomenon suggests that the parallel IGBT chips could be stressed at different level during short circuit, which will be further studied by both simulations in Chapter 4 and experiments in Chapter 5.

3.3.2 Case Study II: Short Circuit in case of Bond Wire Lift-off

When the bond wires fatigue happens, the degraded emitter bond wire has poorer contact and higher electrical resistance than the other bond wires. In this case study, the emitter resistance network is set as follows: the most-left bond-wire in Figure 3.4(a) have tens of kΩ contact resistance, which represents a bond wire lift-off, while the normal bond wire contact resistance is at mΩ level. To compare the results with a new module,

all other settings in PSpice and Icepak are kept the same as the simulation for the new IGBT.

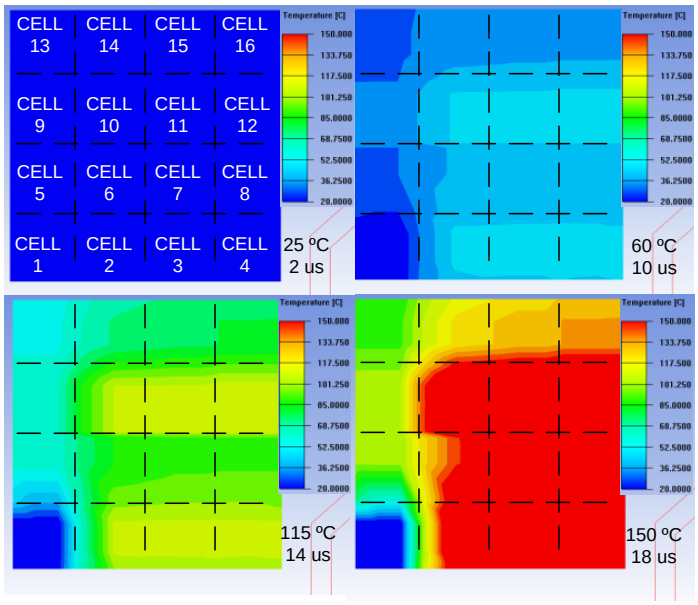

Figure 3.10: *IGBT power module chip temperature maps in Icepak during short circuit at 2/10/14/18 µs in case of one bond wire lift-off (temperature color bar – max 150 °C, min 20 °C).*

The collector current rises rapidly until reaching the saturated current when the short circuit happens. Due to the lifted bond wire on the top, the current distribution among the cells is redistributed, of which the cell 1 conducts almost zero current flow due to the lifted bond wire as illustrated in Figure 3.9. Meanwhile cells 2-4 with fine wire connections carry high current at the beginning of short circuit. At the same time, some differences can be identified among the cells 2-4, which are due to the strongly-involved dynamic temperature variations.

During short circuits, the unequal temperature map is effectively predicted in the thermal simulations, as shown in Figure 3.10. Similar to Figure 3.7, four chip temperature maps during short-circuit are reported in Figure 3.10. They are before short circuit (at 2 μs), during short circuit (at 10 μs and 14 μs), after short circuit (at 18 μs) respectively.

Starting from room temperature (25 °C) (the first picture at 2 μs), the chip temperature becomes unequal during the short circuit. Cell 1 under the lift-off bond wire, is much cooler than the other cells. Cells under well-contacted bond wires (cells 2-4 and cells 10-12) show higher temperature than the others, especially compared with

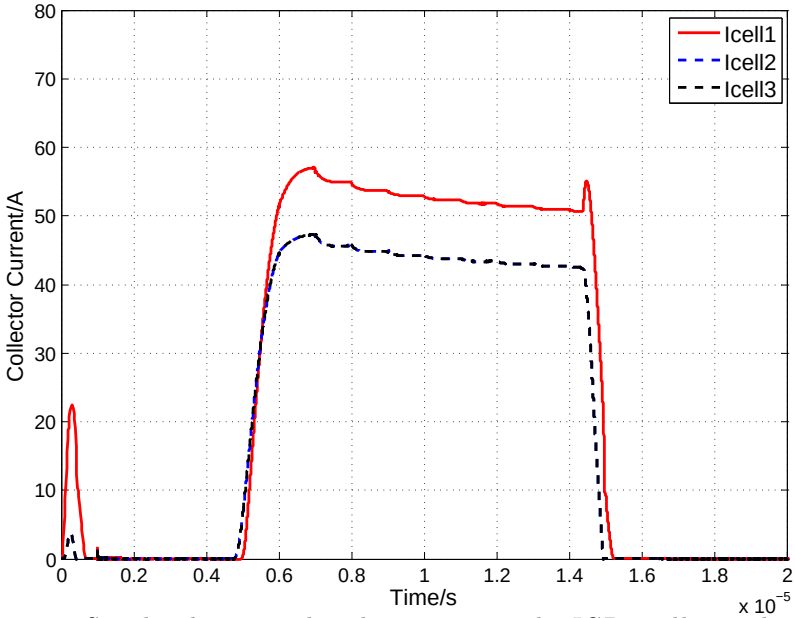

Figure 3.11: *Simulated current distribution among the IGBT cells 1-3 during short circuit in case that cell 1 has a V_{th} degradation.*

the degraded ones. Comparing with the results of the new module in Figure 3.7, the temperature of the non-degraded bond wires is more than 5 °C higher in Figure 3.10. The bond wire lift-off phenomenon will cause remain bond wires carry more current than the new condition, which can accelerate the degradation of the remaining bond wires.

3.3.3 Case Study III: Short circuit in case of Threshold Voltage Degradation

As mentioned before, the proposed electro-thermal co-simulation method has been used to simulate the imbalances among the cells in the chip. Due to the aging and/or stresses in the real lifetime of the module, degradations and deviations of electrical parameters (e.g., gate resistance R_G, and threshold voltage V_{th}) are common among several cells inside the IGBT chip.

Previous research has shown that the threshold voltage shift is a common degradation for MOSFETs and IGBTs [82], [83]. The hot electron injection can lead to positive shift of V_{th}. Instabilities (for instance thermal runway) can be generated afterwards. A previous study has shown the variation of V_{th} is a reliability issue for the parallel-

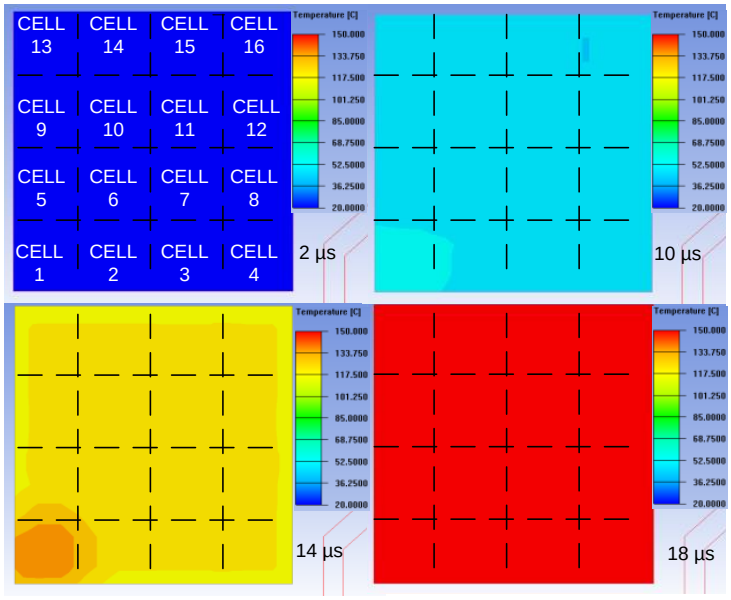

Figure 3.12: *IGBT power module chip temperature maps in Icepak during short-circuit at 2/10/14/18 µs in case of V_{th} degradation in cell 1 (temperature color bar – max 150 °C, min 20 °C).*

connected IGBTs. The IGBTs having lower V_{th} can fail earlier due to larger current (and hence larger power dissipation) at a given bias point [84].

A case study of V_{th} imbalance inside IGBT chip is given here. In the PSpice model, the V_{th} of the lower-left-corner cell (cell 1) is about 2 V lower than the other cells due to critical degradations, which further leads to imbalanced short circuit currents among the cells. The degraded cell carries more current than the other cells, leading to a higher temperature. Simulated currents of degraded cell (cell 1) and non-degraded cells (cell 2 and 3) are plotted as solid line and dashed lines respectively in Figure 3.11. It can be seen that cell 1 carries higher current during the short circuit. Consequently, there is an imbalanced temperature distribution among the cells. After 14 μs, a hot spot is formed as shown in the temperature map in Figure 3.12, implying that thermal runaway can happen due to the V_{th} degradation. Electrical degradation can cause more thermal stress to the DUT, as the simulation results show that the chip temperature is more than 10 °C higher than the new condition in Figure 3.7.

3.4 Summary

A new electro-thermal co-simulation approach involving PSpice and ANSYS/Icepak has been proposed. It exhibits the capability of predicting the current and temperature distribution inside the IGBT chip. Through the case study on a new IGBT module, the approach has predicted the current as well as the temperature distribution under short circuit operations. Further case studies on aging effects like the bond wire lift-off and V_{th} degradation have also been studied with the proposed approach. It is worth mentioning that, the proposed method enables to predict the effects of fatigue and/or degradation under severe conditions, which on the contrary are not straightforward to be experimentally studied.

Chapter 4

Electro-thermal Modeling of the Commercial IGBT Power Modules

This chapter applies the proposed co-simulation method from Chapter 3 to the multi-chip IGBT power modules. Through case studies on the 1.7 kV/ 1 kA IGBT power modules, the co-simulation tool successfully predicts the short circuit current sharing and the temperature distribution among the parallel IGBT chips.

4.1 Information of the Studied 1.7 kV/ 1 kA IGBT Power Modules

4.1.1 Outline and Specifications of the Power Modules

The study is based on the commercial 1.7 kV/ 1 kA IGBT high modules, which are widely used in wind turbine systems, motor drives and other high power converters. The main specifications of the module are summarized in Table 3.3 (on page 41): the maximum operation temperature is 150 °C, the typical collector-emitter saturation voltage ($V_{CE,sat}$) is 2 V, the threshold voltage is 5.8 V. The module has a high DC stability, high current density, and a relatively low switching loss/ conduction loss.

The packaging outline is shown in Figure 4.1(a). The upper IGBT gate terminals are on the right side in Figure 4.1(a), and the lower IGBT gate terminals are in alignment with the terminals of a Negative Temperature Coefficient (NTC) thermistor. There are two power terminals for the DC plus connections (upper IGBT collector), two power terminals for the DC minus connection (lower IGBT emitter), one terminal with two

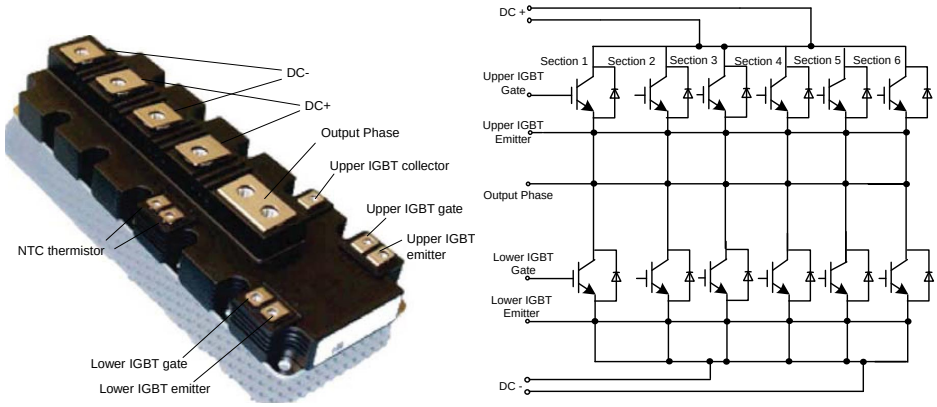

Figure 4.1: *Information of the studied 1.7 kV/1 kA power module: (a) a packaging outline picture; (b) internal structure of the power module with sections definition.*

screw connections for the output phase. The module packaging outline size is 234 mm by 89 mm by 38 mm. There are six sections connected in parallel to increase the current capability, and the definition of section numbers in this study is shown in Figure 4.1(b): the nearest section to the gate pads is defined as section 1, while the farthest section to gate pads is called section 6. Each section contains two IGBT chips and two freewheeling diode chips, which are configured as half-bridge for the standard applications.

The cross section structure of the studied modules is the typical structure of the power modules, as shown in Figure 1.5(c) (in page. 5). The module exterior consists of a plastic frame with screw connections and a metallic baseplate. The plastic frame is mechanically stable, and has high tensile strength within the whole temperature range. It is also electrically insulating, and ensures a long creepage distance at its surface. The silicone gel inside has very good electrical insulation properties. The high power IGBT modules have a copper baseplate to provide fine thermal connection to the cooling medium. The Direct Copper Bonding (DCB) substrate consists of a ceramic dielectric insulator with copper bonded to it. The DCB provides electrical insulation between the potential of the power devices and the potential of the heat sink. It also provides a good thermal connection to the heat sink. The upper copper layer of the DCB consists of copper tracks. The metallic backside of the IGBT chip, the collector side, is soldered directly onto these copper tracks. Bond wires on the top of the chip provide electrical connection to the gate and emitter contact of the chip. Aluminum (Al) bond wires are widely used, and the number of bond wires is eight or ten for different manufacturers.

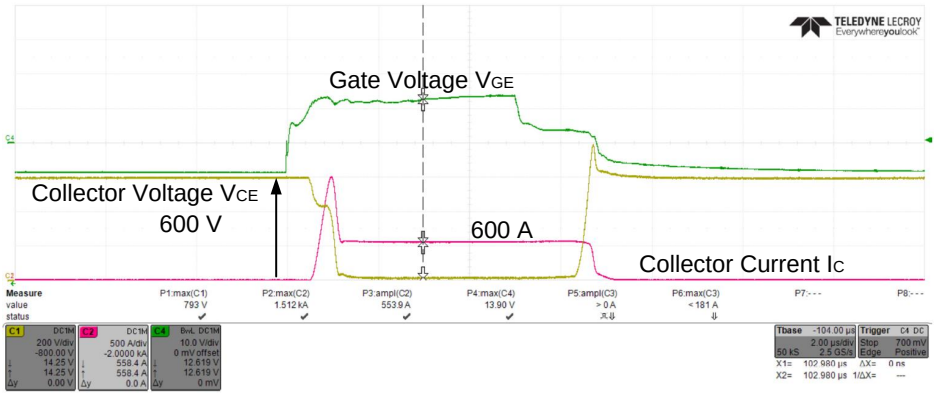

Figure 4.2: *Double pulse testing waveforms for 1.7 kV/1 kA module at 600 V DC voltage. time scale: 2 µs/div; collector voltage (C1): 200 V/div; collector current (C2): 500 A/div; gate voltage (C4): 10 V/div.*

4.1.2 Stray Parameters inside the Power Module

Inside the studied IGBT power modules, multiple chips are connected in parallel to increase the current rating. However, due to the chip characteristics as well as the layout design of the module [11], there could be a considerable current difference among the paralleled IGBT chips. This challenge becomes even more critical for the MW-scale IGBT modules, due to the high current ratings (typically kA-level) and asymmetric geometry. The imbalanced current sharing among the paralleled chips caused by the stray parameter differences can be a reliability critical issue, because the consequent imbalance of temperature will stress the chips at different levels and lead to a lifetime mismatch among different chips.

In the prior-art research, plenty of methods have been addressed on overcoming the stray parameters mismatch among parallel connected IGBT power modules in order to construct reliable high current converters, such as by designing bus bars with consideration of current coupling effects to minimize the stray parameters difference [85], [86], or by synchronizing the IGBT switching signals to trigger IGBTs simultaneously [87], as well as adjusting the gate voltages and the gate resistances based on the thermal imbalance [88], [89]. However, these methods can hardly be applied in high power module constructions, where a unique gate lead is connected to several sections of the module [90]. An electromagnetic field analysis has been applied in [91] to investigate the current differences among 6 parallel IGBT chips based on a detailed structure description, while the mechanisms leading to this current difference have not been discussed. A Partial Element Equivalent Circuit (PEEC) method has been applied to analyze the stray parameters of an IGBT module with 2 or 4 chips in parallel [92], [93], which shows

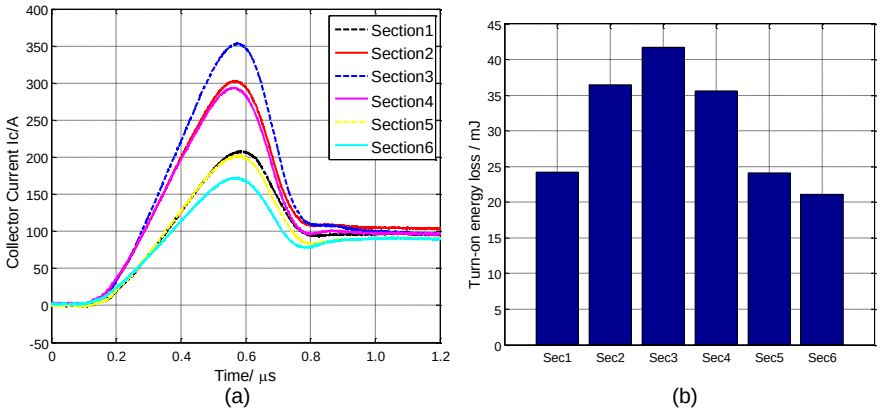

Figure 4.3: *Tests of 1.7 kV/1 kA module A at 600 V DC voltage: (a) measured current distribution among six sections during turn-on transient; (b) measured turn-on energy loss distribution among the six sections.*

that stray parameters extracted at specific frequency cannot reflect both the transient and on-state electrical behavior. The proposed lumped element equivalent resistance and inductance ladder can be used for predicting the electrical behavior inside the module [94], which needs fitting of hundreds of parameters; therefore it is quite time consuming. A recent study on medium power module shows that the module stray parameters difference can affect the power losses and temperature distribution among the parallel IGBT chips [95]. Therefore, it is important to identify the stray parameters inside the MW level IGBT power module at different frequencies, and experimentally study the effects on the current distribution.

Double pulse tests have been performed for two 1.7 kV/1 kA power modules from different manufacturers (module A and B) to show the internal stray parameters effects on the electrical behavior. As is well known, the stray parameters imbalance among the parallel sections can lead to current imbalance during the switching transient. The freewheeling diode's reverse recovery current can lead to a current peak during the IGBT turn-on transient, which can be used for investigating the imbalance. In order to clearly demonstrate the current imbalance, the anti-parallel diode in a 3.3 kV IGBT power module is adopted as freewheeling diode to achieve high current peak.

Figure 4.2 shows the experimental waveforms of the module A, where the collector voltage is 600 V. In Figure 4.3(a), the current distribution among the six sections of module A is further plotted, which has been measured by means of an equal number of Rogowski coils. A non-perfect current balance among the six sections can be recognized especially during the turn-on transient. It can be seen that sections 2-4 conduct more current than the other sections. Figure 4.3(b) gives the calculation of different sections

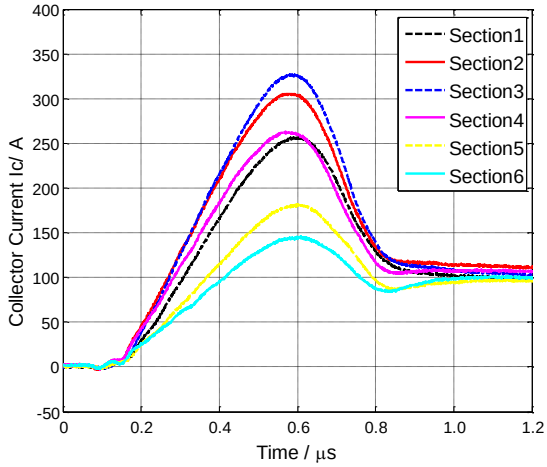

Figure 4.4: *Measured current distribution among six sections of the 1.7 kV/1 kA module B at 600 V DC voltage.*

energy loss during the turn-on transient of Figure 4.3(a). The turn-on loss of section 3 is almost twice of section 6.

In order to check whether the observed current imbalance phenomenon is consistent among different packaging technologies, another IGBT power module (module B) with the same ratings but from a different manufacturer has been tested at the same conditions. Even though module A and B have the same outline and connection, they have different internal structure and geometry. Tests at the same conditions are applied on module B, and the inside current distribution during turn-on is plotted in Figure 4.4. By comparing Figure 4.3(a) and Figure 4.4, it can be seen that the current distribution is slightly different from module A due to the internal design difference. For both modules, the middle sections are slightly more stressed than the lateral ones. The similar current distribution reveals that the internal stray parameters can affect the current sharing among the parallel IGBT chips. It is worth pointing out that the stray parameters can have a bigger influence on the power module behavior under abnormal conditions, for instance during short circuits, because of high dynamic electrical transients (i.e., high di/dt). The short circuit behavior of the studied modules will be the foucs in the following sections.

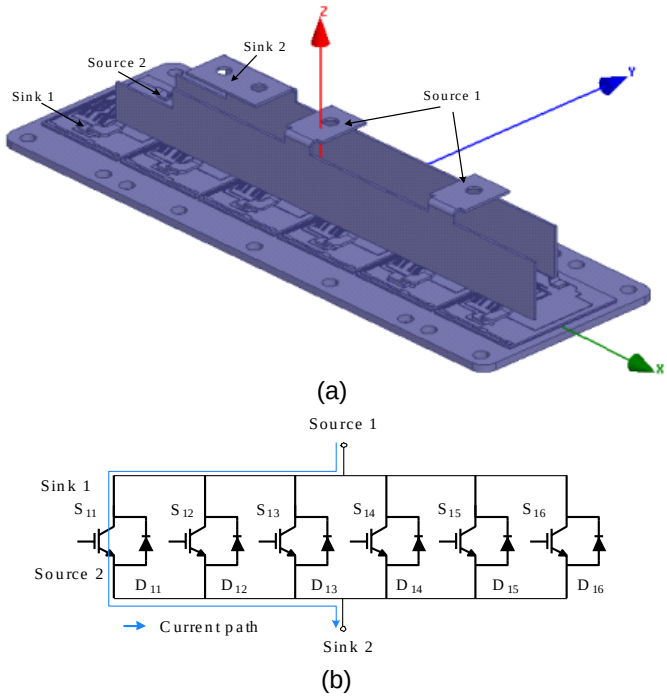

Figure 4.5: *Extraction of stray parameters by Q3D analysis: (a) studied IGBT power module geometry; (b) circuit diagram of the upper IGBTs for showing Q3D analysis, where the current path through the section 1 is given.*

4.2 Case Study I: Short circuit Behavior with Imbalanced Stray Parameters among Parallel Chips

In this section, a 3-D electromagnetic field simulation is integrated into the proposed electro-thermal simulation method. The analysis process has been illustrated in Figure 3.3(a)(on page 37). First of all, the 3-D simulation tool, ANSYS/Q3D Extractor calculates the parasitic parameters of frequency-dependent resistance and inductance of the studied power module structures. Then further studies on the short circuit current distribution among the parallel sections is carried on by the PSpice-Icepak co-simulation method.

4.2.1 Extraction of the Stray Parameters

The Q3D analysis applies Finite Element Method (FEM) and Method of Moments (MoM) [96] to extract the stray inductance and resistance. The Q3D Extractor [97] efficiently performs 3-D and 2-D electromagnetic field simulation of electronic structures based on the mechanical or electrical (layout) CAD data.

Table 4.1: *The stray resistance and inductance of each section's power stage at different frequencies.*

Frequency	**Parameters**	**Section 1**	**Section 2**	**Section 3**	**Section 4**	**Section 5**	**Section 6**
1 kHz	L_x (nH)	74	46	35	48	69	90
	R_x ($\mu\Omega$)	342	225	179	213	264	346
10 kHz	L_x (nH)	72	44	34	46	65	86
	R_x ($\mu\Omega$)	568	323	208	287	400	611
100 kHz	L_x (nH)	70	43	33	44	62	82
	R_x ($\mu\Omega$)	1449	850	469	665	931	1559
1 MHz	L_x (nH)	69	42	33	43	61	81
	R_x ($\mu\Omega$)	4301	2633	1524	1942	2711	4604
5 MHz	L_x (nH)	69	42	32	42	61	81
	R_x ($\mu\Omega$)	10065	6401	4645	5622	7457	10171

At first, a detailed model should be constructed in the software, which should include the geometry and material information. A detailed geometry of the studied IGBT module is created in a CAD program and then imported to the commercial software ANSYS/Q3D. The structure built in Q3D is shown in Figure 4.5 (a), where the sources and sinks assigned are also indicated. Then ANSYS/Q3D uses FEM and MoM to extract resistance, inductance and capacitance matrices. The upper leg of the half-bridge module is studied in this paper (as shown in Figure 4.1(b)). Simulations are performed in Q3D at different frequencies (1 kHz - 5 MHz), and the stray inductances (Lx) and resistances (Rx) of six sections (from the power terminals to each section) are extracted, as shown in Figure 4.5(b). The simulations are done in such a way that, when extracting the inductance and resistance of a certain section, only the IGBT chip of this section conducts. For example, the current path is shown in Figure 4.5(b) for the case when the parameters of section 1 are extracted and S_{11} (the section number is indicated by the second number of subscript) conducts. The simulation results at different frequencies are summarized in Table 4.1.

It is worth noting that simulations should be performed at each frequency separately instead of the "frequency sweep" available in Q3D. This is because the finite element mesh for the adaptive solution is optimized for the simulated frequency only, so the accuracy of the results could vary at frequencies significantly far away from this solution

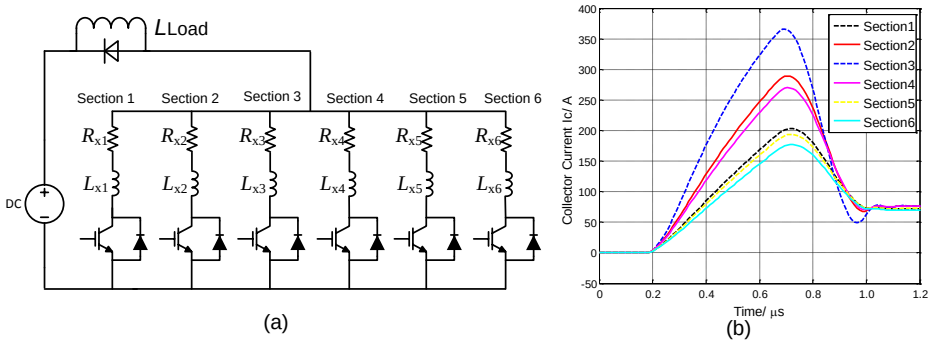

Figure 4.6: *Simulations of the stray parameters effects inside the 1.7 kV/1 kA module: (a) PSpice circuit. (b) simulated current distribution among six sections.*

frequency.

The differences in the inductances and resistances of different sections are observed. The results show that the middle sections (section 2-4) have lower stray inductance and stray resistance than the other sections. It is noted that the stray inductance is almost constant with frequency, while the stray resistance increases with frequency rise due to skin and proximity effects. The imbalance of stray resistance is also higher at 5 MHz than 1 kHz. It means that the current imbalance can be more obvious during the transient, and particular sections may be more stressed and fail first under high frequency operations.

In order to validate the extracted stray parameters, further PSpice simulations are conducted. Figure 4.6(a) shows the simulation circuit, where the stray inductance and resistance of each section are included. The parameters of the components are estimated from the geometry of the physical module obtained by the aforementioned ANSYS/Q3D calculations. The adopted IGBT model is the lumped charge IGBT model. The circuit load inductance L_{Load} is 84 μH, and the freewheeling diode parameters are from the datasheet. Figure 4.6(b) shows the turn-on waveforms under 600 V DC voltage. Comparing the simulation results in Figure 4.6(b) and the experimental results in Figure 4.3(a), the accuracy of the extracted stray parameters are validated. It is noted that the stray parameters are closely related to the operating frequencies. For studying the electrical behavior (e.g., the current sharing) during the conduction state, the parameters at a lower frequency should be used.

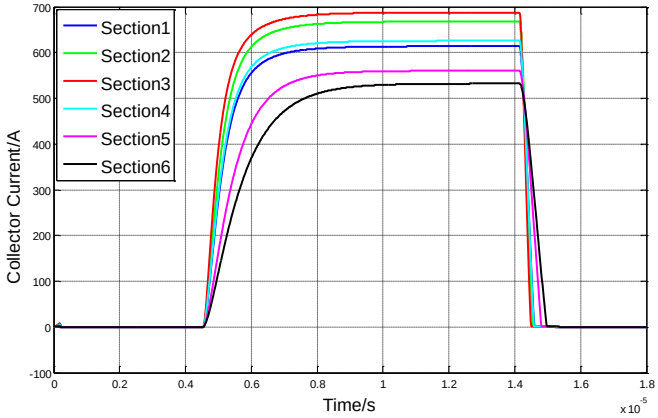

Figure 4.7: *Collector current waveforms among the parallel sections during the 900 V/10 µs short circuits in a pure PSpice simulation.*

4.2.2 Co-simulation Profile Definition for the 1.7 kV/ 1 kA Module

With the extracted stray parameters, a pure PSpice simulation is performed for the 1.7 kV/ 1 kA power module. The electrical profile is: V_{GE} pulse with the amplitude of 15 V, pulse length of 10 μs, DC voltage of 900 V. The simulated short circuit current waveforms are shown in Figure 4.7. The short circuit current is constant, as a constant temperature is used during the simulations. The electro-thermal co-simulations are needed to accurately simulate the electrical behavior during short circuit.

First of all, the electrical simulation circuit is defined in PSpice. The simulation circuit is similar to Figure 4.6(a), where the freewheeling diode is removed and the load inductance L_{Load} is replaced by the circuit stray inductance L_{stray}. The value of L_{stray}

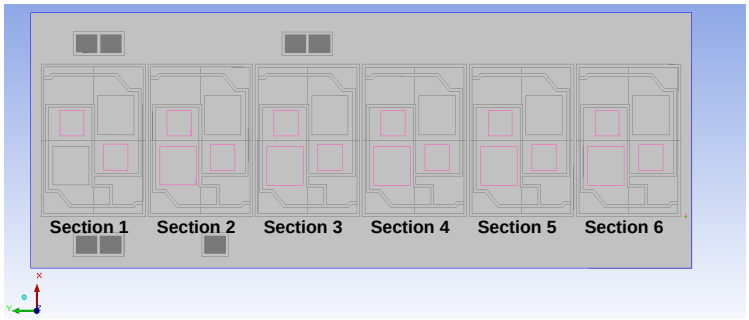

Figure 4.8: *Geometry information of the studied 1.7 kV/1 kA IGBT module.*

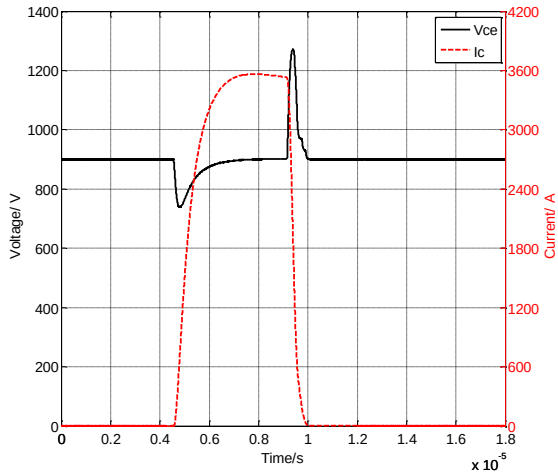

Figure 4.9: *Simulated 900 V/5 μs short circuit waveforms for the 1.7 kV/1 kA IGBT module.*

is 37 nH. The electrical profile is: V_{GE} pulse with the amplitude of 15 V, pulse length of 5 μs, DC voltage of 900 V.

Secondly, the thermal model is constructed in ANSYS/Icepak. The geometry information of the 1.7 kV/1 kA module in Icepak is shown in Figure 4.8. It contains 6 identical sections in parallel. The detailed geometry of one section is plotted in Figure 3.5(on page 40).

4.2.3 Electro-thermal Co-simulation Results of Short Circuit Behavior

When a short-circuit happens during IGBT turn-on (at 4.5 μs), the collector current I_C rises rapidly until reaching the saturated value of 3500 A. It is noted that the rated current is 1 kA for the studied IGBT module. Due to the high di/dt current slope and the stray inductance, there is a voltage drop during the short-circuit turn-on at the collector-emitter voltage. The electro-thermal co-simulation results are plotted in Figure 4.9. The voltage overshoot during the short circuit turn-off is also because of the high current slope di/dt and the stray inductance. It is worth noting that the I_C curve is not obviously decreasing within the 5 μs, which cannot be simply explained by the short testing duration. Suggested by the electro-magnetic analysis results in section 2.1, the above observation can be caused by the parallel sections have different stray parameters.

The simulated short circuit current waveforms of the parallel sections are further plotted in Figure 4.10. An uneven current distribution among the six sections can be

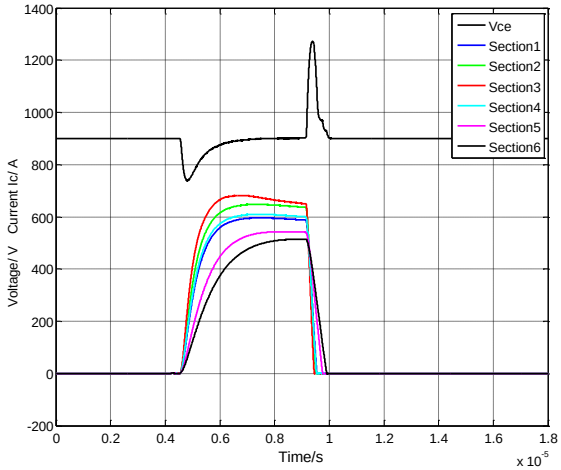

Figure 4.10: *Simulated current distribution waveforms among six sections of the 1.7 kV/1 kA module under the 900 V/5 µs short circuit.*

observed. It is worth noting that section 5 and section 6 have lower *di/dt* during the turn-on transient and the currents through them increase with time. On the other hand, section 2 and section 3 show an obvious overshoot and their currents decrease with time (same behaviour as the I_C in Figure 3.6). What above proves that, even though the total current is almost constant during the simulation, a transient current imbalance occurs. This phenomenon will be further studied by experiments in Chatper 5.

Figure 4.11(a) gives the mesh profile of the DUT, while Figure 4.11(b) shows the junction temperature distribution among the parallel IGBT chips at the end of the V_{GE} pulse, where some temperature differences can be found: the temperatures of middle sections (i.e., section2 and section3) reach about 200 °C, and the temperature of section 6 is about 150 °C. Temperatures of middle sections (i.e., section2 and section3) are higher than the farthest sections to the gate terminals (i.e., section5 and section6). This phenomenon suggests that the parallel chips can be stressed at different level during short circuit.

4.3 Case Study II: Short Circuit Behavior under Uneven Initial Temperatures among Parallel Chips

4.3.1 Co-simulation Profile Definitions

For high power applications, it is necessary to use heatsink and water-cooling systems for the MW-level IGBT modules (e.g., the studied 1.7 kV/1 kA module). The parallel chips

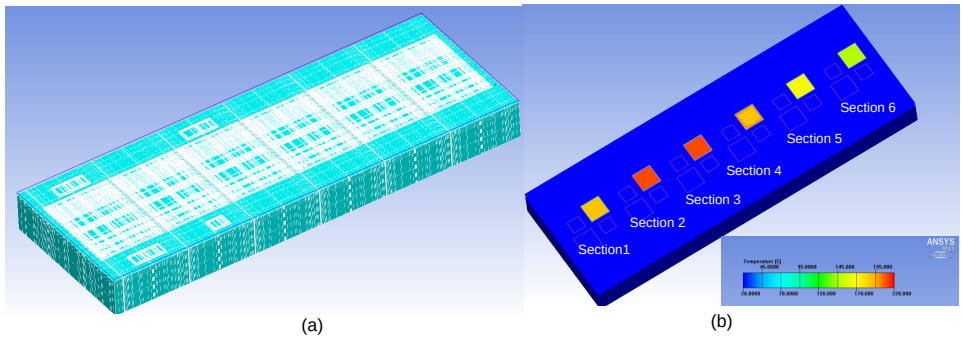

Figure 4.11: *Simulations of IGBT module under short circuit: (a) the mesh profile; (b) simulated temperature profile at the end of the short circuit pulse(temperature color bar – max 220 °C, min 20 °C).*

can have uneven temperature distribution under steady-state because of the imbalanced water temperature power loss distribution. In this case study, the proposed method will be used for studying the IGBT module short circuit behavior under such condition. There are two steps: first a pure thermal analysis to obtain the uneven temperatures among the parallel chips, secondly an electro-thermal analysis afterwards.

For the first step, a boundary condition is selected based on a practical heat transfer coefficient value for the heat sink (data from the water cooling system manufacturer). According to the experimental results in Figure 4.3 and Figure 4.4, a non-perfect current distribution among the six sections can be recognized especially during the turn-on transient. A further comparison of the turn-on energy loss is illustrated in Figure

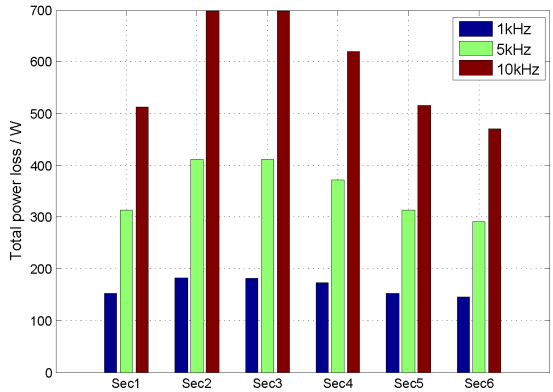

Figure 4.12: *Total power loss (including switching loss and conduction loss) among six sections at different switching frequencies.*

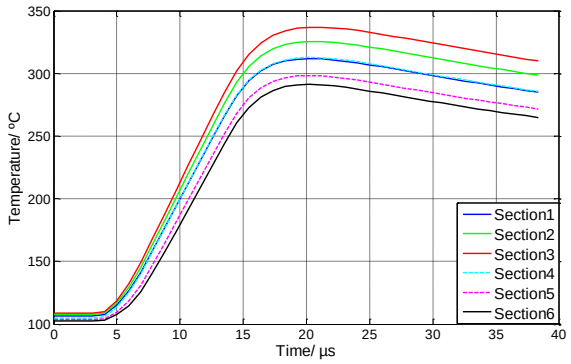

Figure 4.13: *The IGBT chips junction temperatures during short circuits - starting from uneven initial temperatures.*

4.3(b). It can be seen that middle sections (2,3,4) have higher losses than the others. The obtained result could be used for calculating the loss distribution among the parallel sections. As the current during turn-on transient is more imbalanced than the current during on-state, it suggests that different loss distributions can be observed at different operating frequencies. In order to better investigate the frequency effects, a study case is proposed where the IGBT module is operated at different frequencies (i.e., 1 kHz, 5 kHz and 10 kHz) with a duty cycle of 50%. The total power loss (including switching loss and conduction loss) of the sections has been measured and reported in Figure 4.12. At higher operating frequency, the total power loss increases significantly. The power loss distribution at 1 kHz is selected for the first step thermal analysis. With the power loss applied to the parallel chips, the Icepak simulation is running until the steady state – when the junction temperatures reach steady value. There are about 5 °C differences among the chips junction temperatures as shown in Figure 4.13 (t=0 s). At this point, all FEM data is saved for the second step.

For the second step: the steady-state FEM data is loaded as the restarting point for thermal analysis. The short circuit profile is: V_{GE} pulse with the amplitude of 15 V, 10 μs pulse length, 900 V DC voltages. The electro-thermal analysis starts from the uneven initial temperatures.

4.3.2 Co-simulation Results

The simulated junction temperature distribution among parallel chips is shown in Figure 4.13. It can be seen that the temperature of section 3 is the highest, while the temperature of section 6 is the lowest, which is consistent with the previous analysis. The mismatch between the temperature curves increases with the time and the difference is already 20 °C at 5 μs after short circuit beginning (t=10 μs in Figure 4.13). At the end of the short circuit pulse the temperature mismatch is 50 °C.

4.4 Summary

This chapter firstly analyzes the stray parameters inside the commercial high power IGBT modules, and then applies the proposed electro-thermal co-simulation approach to study the current and temperature distribution among the parallel IGBT chips. Case studies on the 1.7 kV/1 kA IGBT modules show that the approach can predict the current as well as temperature distribution under short circuit situation.

Chapter 5

Electro-thermal Model Validation by means of Non-destructive IGBT Tests

This chapter discusses the experimental validation results in order to prove the effectiveness of the proposed approach. A 1.1 kV/ 6 kA non-destructive testing facility is described, which has been built up at CORPE, Aalborg University. Simulated electrical behavior during short circuits in Chapter 3 and Chapter 4 has been verified with measurements.

5.1 Description of 1.1 kV/6 kA Non-destructive Tester

5.1.1 Structure and Operating Principle

The IGBT short circuit withstanding capability is an important parameter for both the application engineers and also the manufacturers of the modules. Plenty of research efforts have been devoted to the study of the short circuit capability of IGBTs. In [98], the short circuit current capability is studied by the repetitive low-energy-level short circuit tests. It reveals that the repetitive low-energy-level short circuit can cause the Al metallization layer degradation and the on-state resistance increasing. In [99], a "critical energy (E_C)" is proposed to explain the mechanisms of IGBT failure under repetitive short circuit operations. When the short circuit dissipated energy is below E_C, IGBT may survive for more than 10^4 times repetitive short circuit operations. However, when short circuit energy is beyond E_C, the IGBT may fail after the first short circuit because of thermal runaway. A further experimental investigation shows that the IGBT can

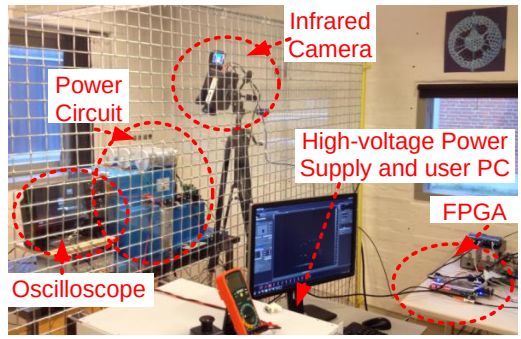

Figure 5.1: *Picture of the high current Non-Destructive Tester (NDT).*

turn off short circuit successfully, but fails after several microseconds when the short circuit energy is slightly higher than E_C. It is still challenging to determine the exact value of E_C, even though many experiments and numerical simulations have been done previously [51]. Traditional short circuit testing equipment includes the Device Under Test (DUT), a set of capacitors and a circuit breaker in series, where an over-current detection is also integrated in order to avoid the DUT explosion and allowing post-failure analysis [98], [99].

Recently, several non-destructive testing concepts have been proposed to perform repetitive over-current and short circuit testing of IGBTs, while avoiding significant device damage. The implementation of non-destructive testing systems for discrete IGBTs (up to 100 A) and for higher power IGBT modules (up to 2.4 kA) were discussed in [100], [101]. The main focus was to study the IGBT short circuit behavior at various electrical conditions. It is a very cost-effective way especially for testing high power IGBT modules. In this chapter, the short circuit study of high power IGBT modules is performed on a state-of-the-art non-destructive tester (NDT) with the current and voltage limits of 6 kA and 1.1 kV.

The basic principle of the non-destructive testing technique is to perform repetitive tests up to the physical limits of the DUT, while avoiding device destructions, even in case of device failure. This characteristic is particularly desirable as it permits post-failure analysis in the case of device rupture. At the same time, the technique presents challenges due to requiring one or more additional protection switches, typically put in series to the DUT. These switches have higher nominal voltage and current ratings and should not alter the overall circuit inductance significantly. A high-voltage power supply (as shown in Figure 5.1) charges up preliminarily a capacitor bank C_{DC} to a specific testing voltage. This capacitor bank supplies all the energy required for the test. A series protection switch is connected between the capacitor bank and the DUT. It is turned on before the short circuit is made and switched off right after the test in

order to save the DUT from possible explosions. The voltage and current rating of the series protection switch is higher than the DUT's. However, careful considerations were made in the design of the busbar [102], [103] and an optimized busbar was developed to minimize the overall circuit inductance. The overall circuit inductance is calculated through the use of a commercial CAD tool (Computer Aided Design tool) and a FEM (Finite-Element Method) software (Ansys Q3D) [97], [104]. The experiments in Section 5.2 confirm that the software estimation is in a good approximation.

In case an open DUT is available, an infrared camera FLIR X8400sc [105] with 3 kHz sampling frequency can also be used to obtain the temperature distribution among the internal chips. A supervising unit, based on the Altera® Cyclone IV FPGA, is used to provide the driving signals for the DUT, the protection switch and the infrared camera. It also provides the precise time control for the electrical measurement with an accuracy of 10 ns. A LeCroy HDO6054-MS oscilloscope is used for the acquisition of the waveforms. A Personal Computer (PC) is the user interface, which is connected to the equipment via an Ethernet link and an RS-232 bus. . Two commercial IGBT drivers from Amantys Corp. [106] and Concept Corp. [107] have been used to drive the protection switches and the DUT respectively. In order to perform short circuits, the protection circuit on the DUT drivers is deactivated. During each short circuit, the collector current, collector voltage and gate voltage waveforms are acquired. Figure 5.1 shows a photograph of the laboratory setup, which is behind a safety cage together with the PC and FPGA board. Behind the cage the power circuit can be identified together with the oscilloscope and the infrared camera.

Table 5.1: *Ratings of the main components in the NDT circuit.*

Characteristic	**Value**
DC Maximum voltage	1.1 kV
DUT Maximum current	6 kA
DC capacitors C_{DC}	5 x 1100 μF, 1100 V
Stray inductance of the main loop	37 nH
Series protection	2 x Dynex DIM1500ESM33-TS000 3 kA/ 3.3 kV
Parallel protection	2 x Mitsubishi CM1200HC-66H 2.4 kA/ 3.3 kV
Auxiliary capacitors C_{NEG}	3 x 1100 μF, 1100 V
Schottky diodes	5 x 170 V, 1.2 kA

A detailed electrical schematic of the NDT is shown in Figure 5.2. Table 5.1 summarizes the specifications of the components. There are several components in parallel to

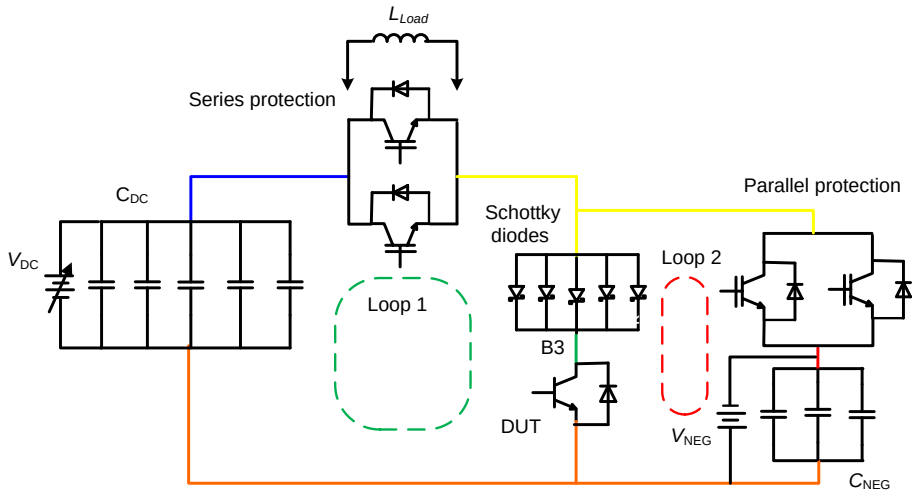

Figure 5.2: *Detailed schematic of the Non-destructive Tester circuit.*

enlarge the current capability and to minimize the stray inductance at the same time. It is worth pointing out that there is an additional leg in parallel to the DUT, where a parallel protection is included together with a capacitor bank C_{NEG} and a battery V_{NEG}. In the same schematic, five Schottky diodes and an optional load inductance L_{Load} are included too. The circuit is divided into two loops: Loop 1 is the main loop including the series protection, while Loop 2 includes the parallel protection. The DUT is located in the common branch. The parallel protection has a twofold role: 1) to assist the series protection during its turn off by diverting the typical tail current of IGBTs, and 2) to act as a crow-bar in case that any instability happens. To enhance its promptness and effectiveness, a negative bias is fed to its emitters by the battery V_{NEG} and the capacitors C_{NEG}. In this way, the typical large voltage tail at the turn on of the IGBT switches is accelerated and the voltage drops to zero more promptly. To prevent supplying negative voltage to the DUT, Schottky diodes are placed in the circuit.

An optional inductance L_{Load} can be placed to perform different types of short circuit. As shown in Figure 5.3, there are mainly two different types of short circuit: A Type I short circuit happens during the DUT turn on, whereas a Type II short circuit happens during the DUT on-state. The NDT can provide both short circuit types by different configurations and control timimg schemes. In case of a Type II short circuit, the inductance L_{Load} is used to simulate the load. The control time schemes for the two types will be illustrated in Section 1.3 of this chapter.

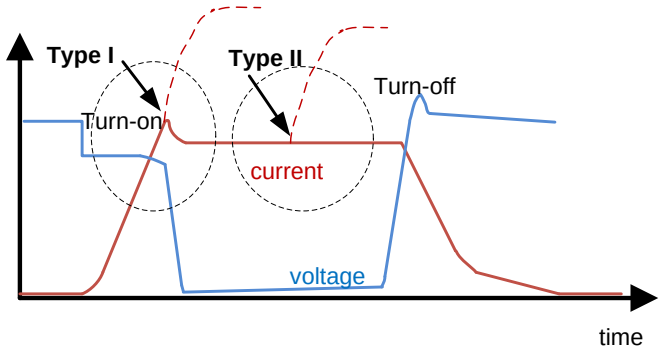

Figure 5.3: *Two possible types of short circuits: the Type I short circuit occurs during turn-on, whereas the Type II short circuit occurs during the conduction state.*

5.1.2 Low Inductance Busbar

The high current slope during turn-on and turn-off under short circuits (i.e., at kA/μs level) necessitates that the stray inductance is kept to a minimum. The busbar design of the NDT power circuit is illustrated in Figure 5.4(a)-(b). Figure 5.4(a) provides a

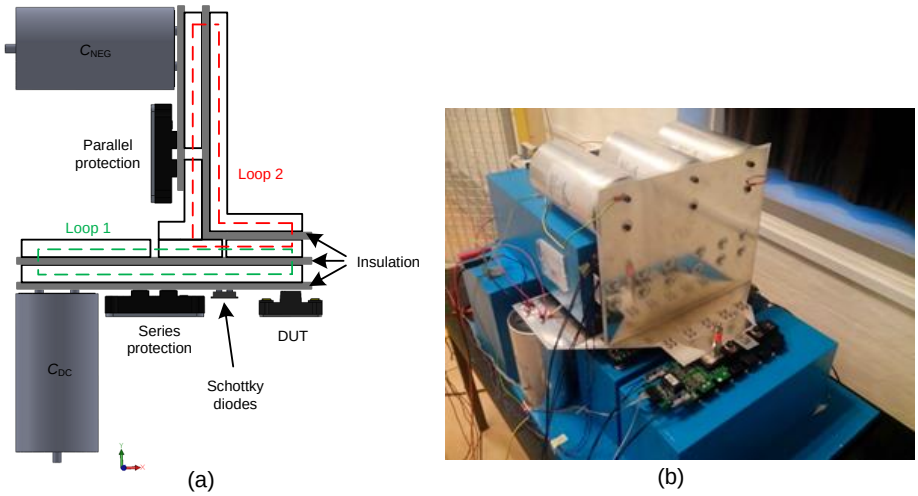

Figure 5.4: *Busbar design of the nondestructive testing circuit. (a) principle cross section of the busbar layers - Loop 1 is the horizontal one, Loop 2 is the vertical one. (b) picture of the final physical prototype.*

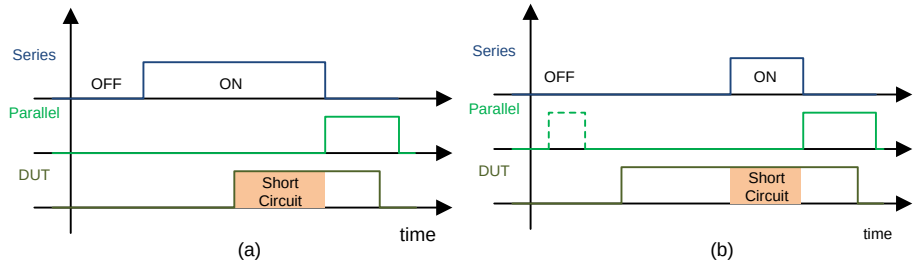

Figure 5.5: *Timing settings for two types of short circuits. (a) timing diagram for Type I short circuit. (b) timing diagram for Type II short circuit.*

cross-section view of the NDT (not to scale): the DUT is the black module in the lower right corner, and the two capacitor arrays C_{DC} (5x) and C_{NEG} (3x) are located under and behind the busbars, respectively. The busbar layers are highlighted with the same layer colors in Figure 5.2. The series and parallel protection are also located under and behind the busbars, respectively. The Schottky diodes are installed in five square windows close to the DUT. The adopted T-shaped geometry allows observing the DUT's temperature distribution from the top with the infrared camera.

A Mylar isolation foil has been used for the busbar dielectric layer. The design of the geometry has been performed with a three-dimensional CAD tool in order to optimize the placement of the components in a way that the mutual coupling among them reduces the overall inductance value. Ansys Q3D was used repeatedly to verify such placement until the best configuration was achieved. The low stray-inductance design has been verified by experimental tests in Loop 1 with a result of 37 nH, including the intrinsic inductances of the series protection and the capacitors. This value is even lower than the theoretical calculations [104]. Figure 5.4(b) illustrates the whole assembly design and the related picture.

5.1.3 FPGA-based Supervising Unit

Short circuits can be classified as Type I and Type II. Type I happens at the device turn on. In this case, there is no need for the load inductance L_{load}, hence it is removed from the circuit. As shown in Figure 5.5(a), the series protection is preliminarily turned on and the parallel protection is turned off. Since Schottky diodes behave almost like ideal diodes, the DUT works as if it were directly connected to the C_{DC} capacitors. The DUT is then turned on, and a short circuit occurs (shadowed period in Figure 5.5(a)). After a given delay, the series protection is switched off and the parallel protection is switched on, and the short circuit waveforms are acquired from the DUT turn on until the firing of the protection. Several tests are performed step by step at increasing delays,

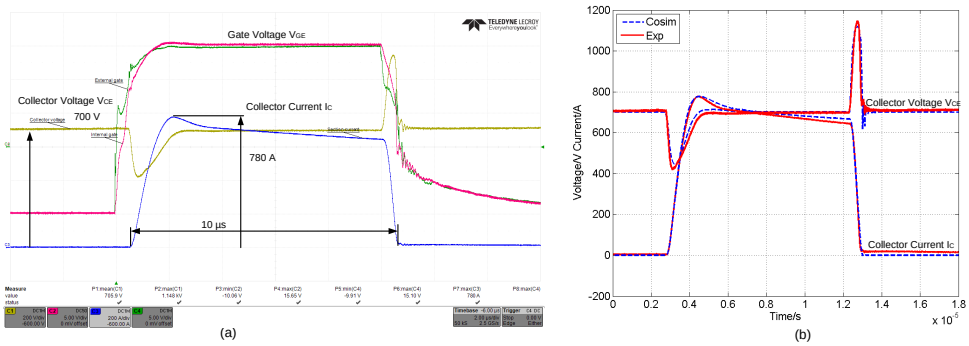

Figure 5.6: *Short circuit of one section inside the IGBT module: (a) experimental waveforms during a 700 V/10 µs short circuit at room temperature 25 °C: time scale 2 µs/div, collector voltage 200 V/div, collector current 200 A/div, gate voltage 5 V/div, (b) comparison between the electro-thermal simulation and the experimental waveforms under the same condition.*

up to the programmed DUT on time. In this way, if any instability begins to occur at a specific step, the sequence is stopped to avoid any damage to the DUT.

Contrarily to Type I, a Type II short circuit happens during the on-state of the device. In this case the inductance, L_{load} is required to simulate the load. Referring to Figure 5.5(b), the parallel protection is turned on first, while the series protection is still off. This preliminary phase is very similar to the double-pulse test concept, where a first pulse is used to magnetize the load inductance [108]. However, contrary to the double pulse tests where the DUT itself is used to such an aim, here the parallel protection is used instead, so any possible self-heating on the DUT is avoided. This can guarantee tests are performed at stable temperatures in the DUT. The series protection diodes operate as freewheeling diodes for the load inductance. Then, the DUT is turned on and a normal commutation happens. After that, the series protection is switched on and a short circuit is induced. After a specified delay, the series protection is switched off and the parallel protection is switched on. Similarly to the Type I short circuit, several tests are performed step by step at increasing delays, up to the programmed DUT conduction time. The above time sequences are generated by an FPGA-based supervising unit, the details of which can be found in [109].

5.2 Short Circuit Electrical Behavior Validation

5.2.1 Experimental Validation of Simulations on One Section

In order to validate the electro-thermal co-simulation results in Chapter 3, the short circuit tests have been carried out at the same condition as the simulations. A 10 μs

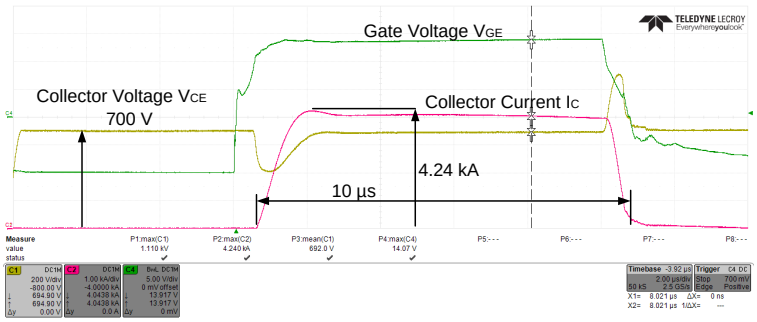

Figure 5.7: *Electrical behavior of the 1.7 kV/1 kA IGBT module during a 700 V/10 µs short circuit: time 2 µs/div, collector voltage 200 V/div, collector current 1 kA/div, gate voltage 5 V/div.*

short circuit test at 700 V for one section inside the studied power module has been performed in the laboratory at room temperature (25 °C). The short circuit current of one IGBT chip reaches 780 A, and decreases along with the time due to the self-heating effects. Experimental collector voltage/ current waveforms are shown in Figure 5.6(a). Due to the test circuit stray inductance, it is observed the collector voltage undershoot and overshoot at the starting and end of the short circuit operation, respectively. It is worth mentioning that the DUT has also been tested at higher voltages, for instance 900 V for 10 μs in Figure 5.9.

The experimental waveforms in Figure 5.6(a) can be used for verifying the electro-thermal co-simulation results in Chapter 3. The simulated waveforms under same condition are plotted in Figure 3.6 (on page 42) by the proposed PSpice-Icepak co-simulation method. A comparison between the simulated and experimental short circuit waveforms is further given in Figure 5.6(b). It shows that the proposed co-simulation method can predict short circuit behavior well, for instance the voltage undershoot and overshoot during the turn-on and turn-off transients, as well as the short circuit current decreasing due to self-heating effects. It can be seen that the simulation and experimental current waveforms match each other well during the turn-on and turn-off. There is a small current difference at the end of short circuit duration, about 25 A, which is within 5%.

5.2.2 Experimental Validation of the Simulations on Power Modules

Thanks to the FPGA controller, the short circuit time duration could be increased or decreased with a step of 10 ns, which provides the possibility of comprehensively investigating the IGBT module short circuit behaviour. The studied 1.7 kV/1 kA IGBT module is further tested under 700 V for 10 μs short circuit at room temperature (25

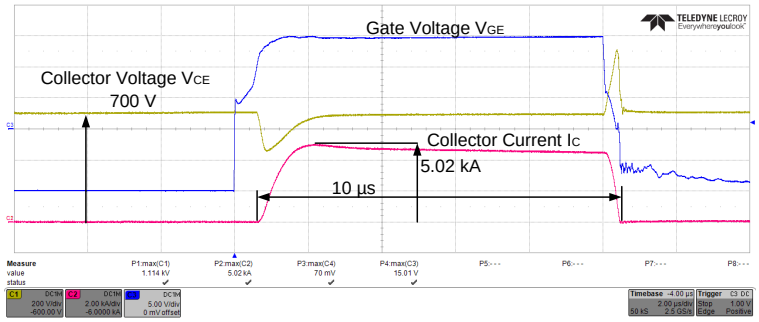

Figure 5.8: *Electrical behavior of the 1.7 kV/1 kA IGBT module from another manufacturer during a 700 V/10 µs short circuit: time 2 µs/div, collector voltage 200 V/div, collector current 2 kA/div, gate voltage 5 V/div.*

°C), the peak short circuit current reaches 4.24 kA. Gate voltage (V_{GE}), collector current (I_C) and collector-emitter voltage (V_{CE}) waveforms during short circuit are shown in Figure 5.7. Similarly to Figure 5.6(a), the collector voltage undershoot during short circuit turn-on and voltage overshoot during short circuit turn-off can be seen. It is worth noting that the current decreasing slope for the whole power module (in Figure 5.7) is slower than the IGBT section (in Figure 5.6(a)). This difference implies that there could be different current values among the parallel IGBT chips during short circuits, as predicted by the simulations in Chapter 4.2. It could be because of the temperature differences among the parallel IGBT chips during the short circuit transient, as well as the stray parameter difference among sections. The current distribution inside the power module will be further studied by means of experiments in Section 5.2.3.

Another 1.7 kV/1 kA IGBT module from a different manufacturer is further tested under same conditions (i.e., 700 V for 10 μs short circuit at room temperature 25 °C). The experimental waveforms are shown in Figure 5.8. It can be seen that the saturated short circuit current for this module is about 5 kA, which is higher than the module tested in Figure 5.7. With sharper turn-on and turn-off slopes of gate voltage, this IGBT module also shows faster turn-on and turn-off behavior than the first module. These differences can be caused by the different chip technology between the two manufacturers.

Another short circuit test has been carried out for the second module with a harsher profile (V_{GE} = 15 V, V_{CE} = 900 V, duration 10 μs), and the experimental waveforms are shown in Figure 5.9(a). The saturated short circuit is 5.2 kA in this condition, which is a little higher than the value in Figure 5.8 – due to the higher collector voltage. Based on the co-simulation structure and process illustrated in Chapter 3, an electro-thermal simulation has been performed for this IGBT module. The simulation profile is same as the experiments (V_{GE} = 15 V, V_{CE} = 900 V, duration 10 μs). Figure 5.9(b) gives

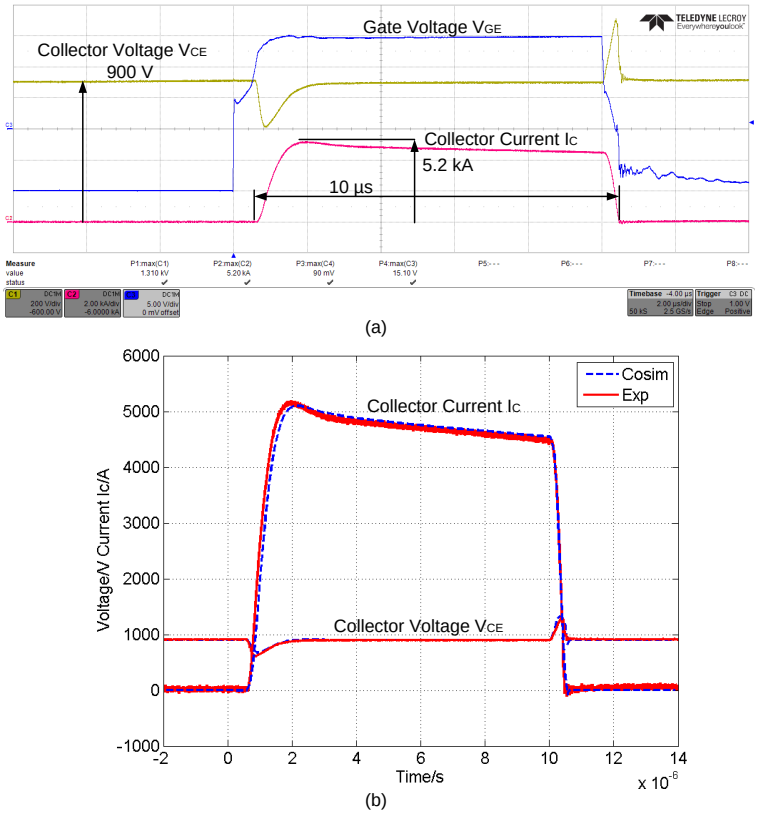

Figure 5.9: *Short circuit of the 1.7 kV/1 kA IGBT module from the second manufacturer: (a) Experimental waveforms at 900 V/10 µs short circuit at room temperature 25 °C: time 2 µs/div, collector voltage 200 V/div, collector current 2 kA/div, gate voltage 5 V/div. (b). Comparison between the electro-thermal simulation and the experimental waveforms under the same condition.*

a comparison between the electro-thermal co-simulation results and the experimental waveforms. It shows that the PSpice-Icepak co-simulation waveforms match the experimental ones well. There is a small collector current difference during the short circuit, where the simulated current is a little higher than experiments (the error is within 3%).

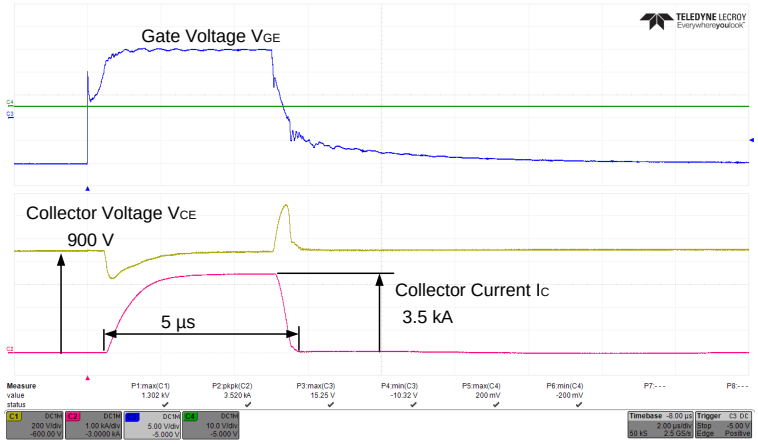

Figure 5.10: *Electrical behavior during a 900 V/3.5 kA/5 µs short-circuit: gate voltage waveform (5 V/div); collector voltage and current waveforms (200 V/div; 1 kA/div; 2 µs/div).*

5.2.3 Experimental Validation of Current Distribution among Parallel Chips

In order to experimentally investigate the current distribution among parallel chips, an open module without silicone gel is tested by means of the NDT. A customized "Ultra mini CWT" Rogowski probe with custom coil length has been adopted for current measurements owing to its non-intrusive behavior (typical impedance in the range of a few pH) and its range of several kA [110].

The open module is tested under 900 V for 5 μs short circuit at room temperature (25 °C). Figure 5.10 gives the collector current and voltage waveforms during short circuit. It is noted that the short circuit current of the DUT is 3.5 kA, and the current is almost constant with the time during short circuit, which are different with the experiments in Figure 5.7 and Figure 5.8. In order to study this phenomenon, further investigations on the short circuit current of each section are carried out. The current distribution among the six sections of DUT has been measured by means of an equal number of Rogowski coils under 900 V/5 μs short circuits.

The short circuit current waveforms are plotted in Figure 5.11. The section number is consistent with the numbers in Figure 4.1(b). It evidences imbalanced short current currents among six sections: the middle sections (2-4) carry higher current than the other sections. The short circuit currents have not achieved steady values for sections which have higher stray parameters (section 5 and 6). Referring to the co-simulation results in Figure 4.10, it can be seen that the imbalance of current amplitude and turn-on slopes among the six sections are well predicted. A further comparison of co-simulation

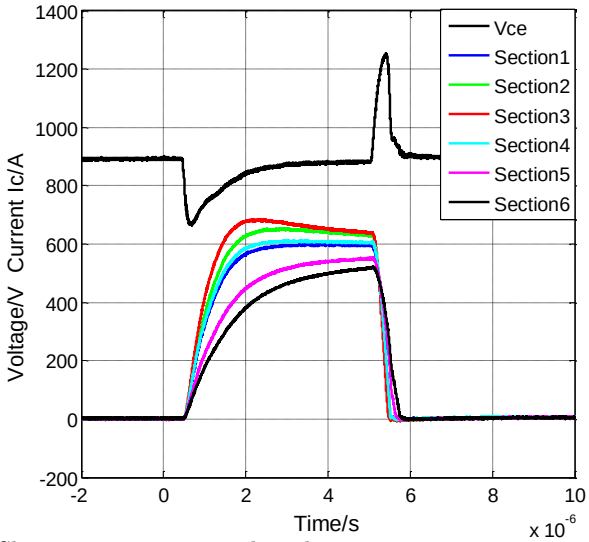

Figure 5.11: *Short circuit current distribution among 6 sections at the same test conditions of Figure 5.10. Lowest short circuit currents flow at the farthest sections (section5 and 6) from the external gate.*

results in Chapter 4 and experimental results of section currents are given in Figure 5.12. It can be seen the proposed electro-thermal co-simulation method can accurately predict the voltage, current waveforms caused by the electrical parameters deviations. Both simulations and experiments show that some chips are more stressed than others

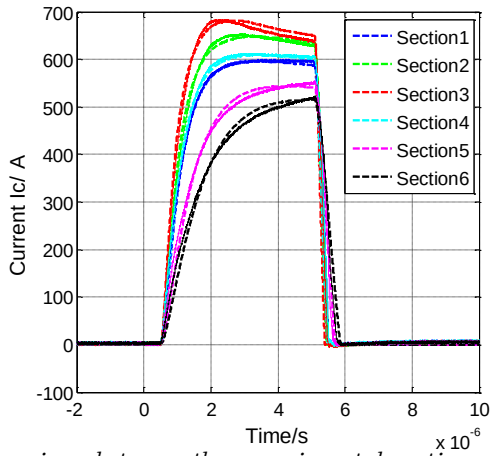

Figure 5.12: *Comparison between the experimental sections currents (solid lines) and the simulated ones (dashed lines) during a 900 V/3.5 kA/5 µs short circuit.*

during short circuits, as well as suggest a dominating effect of the inductance in the imbalance phenomenon. It has been shown that the stray parameters imbalance lead eventually to a non-equal current distribution among the parallel chips. This study can provide a feedback to module designers on optimizing module's internal structure and geometry, as well as give suggestions for application engineers to improve the thermal management and/or cooling system design.

5.3 Temperature Evaluation during Short Circuit

5.3.1 Temperature Sensitive Electrical Parameter Method

It is worth pointing out that the experimental validation of any electro-thermal model in the short circuit regime is very hard because of the fast transients occurring in the temperature distribution (in the range of a few microseconds). Among the several junction temperature (Tj) measurement methods (thermocouples, optic fibers, etc.) infrared cameras are the only ones which can perform up 1 μs shooting time [111], but the low and temperature-dependent emissivity of the metals on the chip surfaces can lead to very inaccurate results [64], [111]. Black-painting the chip surface is a common way to perform infrared measurement, which can give uniform and constant emissivity; at the same time, though, it introduces a low-pass filtering in the thermal response. Another prevailing method is the lock-in thermography technique [111]: the principle is to stimulate the circuit with a sinusoidal signal and to evaluate only the oscillating components of the detected signal at the same frequency and filter out all the remaining noise. The main drawback for testing high power IGBT modules under short circuit with this technique is to repeat such a stressful test (with potential explosions) with no guarantee about device degradation during tests. A similar method is the "equivalent time sampling": the principle is to periodically test the sample, while shifting the acquisition instant by a fixed time each period, to achieve higher sampling frequency than the camera intrinsic frame rate. Even with calibration procedure, the short circuit duration should be very long to obtain acceptable degree of confidence, which may be far beyond the realistic conditions. One recent example is detecting MOSFET transient temperature at low voltage (i.e., up to 30 V) and long short circuit duration (from 60 μs to 10 ms) [112]. Therefore, it may not be feasible to evaluate Tj during realistic short circuit conditions (i.e., several hundred volts, less than 10 μs) of MW-scale IGBT modules by these methods.

Meanwhile, the temperature measurement with temperature-sensitive electrical parameters (TSEPs) has many advantages, such as fast response, as well as no special packaging modifications. Traditional IGBT on-state voltage drop and gate threshold voltage has been employed as TSEPs in thermal impedance characterization [113], which cannot be applied to abnormal operations such as short circuit. It is noted that the short circuit current has a negative temperature coefficient, which is due to the reduc-

Figure 5.13: *Testing setup for IGBT saturation current at different temperatures.*

tion of the transconductance with increasing temperature [46]. The short circuit current depends strongly on the gate voltage, while it is not sensitive to the collector voltage. A recent study tries to apply short circuit current as a TESP for Tj evaluation during the converter operations, which has good selectivity and linearity [114]. It is worth noting that the "junction temperature" obtained in this method can only represent the channel temperature because the short circuit current value is mainly dependent on the device channel temperature. In this work, the short circuit current is adopted to evaluate the Tj during short circuit.

5.3.2 Calibration and Temperature Measurement

In order to represent the relationship between the short circuit current and the device temperature, a calibration is carried out on an IGBT module by means of a curve tracer. Figure 5.13 shows the testing setup for calibration. The DUT is the studied 1.7 kV/1 kA IGBT module. It is worth noting that only one IGBT section is tested to eliminate the effect of imbalanced stray parameters. The curve tracer is the Keysight high power B1506A, which is rated 3 kV/ 1.5 kA. The temperature-controlled hotplate can achieve temperature up to 160 °C with an accuracy of 1 °C. The obtained IGBT

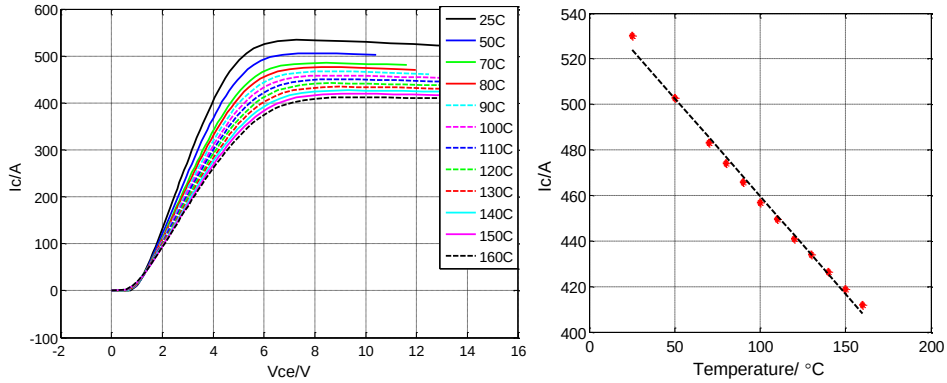

Figure 5.14: *Measurement results: (a) IGBT output characteristics at various temperatures (V_{GE}=15V), (b) IGBT saturation current as a function of temperature (V_{CE}=10V).*

output characteristics at various temperatures (from 25 °C to 160 °C) with the gate voltage at 15 V are shown in Figure 5.14(a). It can be seen that the short circuit current decreases as the temperature increasing. Figure 5.14(b) shows the short circuit current as a function of temperature with V_{CE} at 10 V. The short circuit has an adequate temperature sensitivity of 0.86 A/°C and a good linearity.

The obtained calibration curve can be applied for temperature evaluation during short circuit in Figure 5.6. The testing conditions are: V_{GE} = 15V, 10 μs short circuit

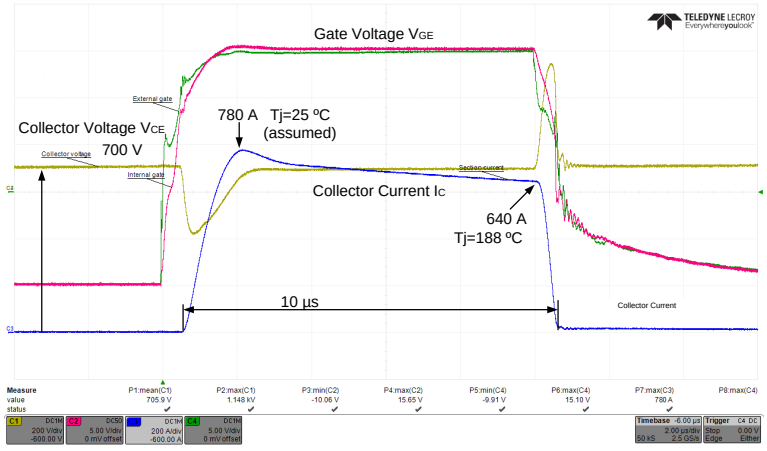

Figure 5.15: *IGBT junction temperature measurement for the tests in Figure 5.6*

duration, $V_{CE} = 700$ V, at room temperature (25 °C). The short circuit current reaches 780 A at 1.5 μs after current starts increasing, and it decreases to 640 A at the end of short circuit (shown in Figure 5.15). According to the calibration curve in Fig. 5.14(b), the junction temperature increases 163 °C during the above points. If we assume the Tj is 25 °C at 1.5 μs (ignored the self-heating effects during the first 1.5 μs), the Tj is 188 °C at the switching off point.

5.4 Summary

In this chapter, a non-destructive tester rated at 6 kA/1.1 kV is used to investigate the short circuit behaviour of MW-scale IGBT power modules. Its main feature is to enable studying instabilities while protecting the device under test against explosions with a time resolution of 10 ns using FPGA hardware. A comprehensive study has been performed on commercial IGBT power modules short circuits. The results verify the proposed PSpice-Icepak co-simulation method's accuracy, as well as suggest a dominating effect of the inductance in the short circuit current imbalance phenomenon. The short circuit current itself has been adopted for extracting junction temperature during short circuits, which has shown a good linearity.

Chapter 6

Conclusions and Future Work

This chapter summarizes the work, which has been done throughout this Ph.D. project, and emphasizes the main contributions of this project – a physics-based electro-thermal simulation tool of the high power IGBT modules and a 1.1 kV/6 kA non-destructive tester for verifying the simulation results. Then, this chapter ends with an outlook of this topic in order to enrich the future research outcomes.

6.1 Conclusions

The main subject of this project was the evaluation and assessment on the electro-thermal behavior of modern power IGBT modules under abnormal conditions, especially during short circuits. The subject has been investigated by means of the proposed physics-based electro-thermal simulation tool described in Chapter 3 and Chapter 4. Further experimental evaluations have been conducted by means of a 1.1 kV/6 kA non-destructive tester in Chapter 5, which also validated the accuracy and effectiveness of the proposed modeling method.

Based on all the work done, the following conclusions can be given:

Co-simulation Approach for IGBTs Electro-thermal Coupling Effects under Short Circuit

An electro-thermal co-simulation approach involving PSpice and ANSYS/Icepak has been proposed, which connects a physics-based, device-level, distributed electrical simulation tool with a thermal FEM simulation, to obtain a high accuracy on both the electrical side and the thermal side. It can adopt independent time steps for the electrical and thermal parts, thus gaining improved calculation efficiency. It has the capability of predicting current and temperature distribution inside one IGBT chip as well as among several parallel IGBT chips under short circuit. It also demonstrates that the

IGBT saturated short circuit current dramatically decreases when the chip temperature increases due to the self-heating effects. The simulation results show that the IGBT junction temperature can be still relatively high for several μs after short circuit, which can explain the phenomenon that IGBT fails at several μs to several tens of μs after successfully turned-off short circuits.

Degrading Effects on IGBT Short Circuit Behavior

Through the case studies, the proposed method predicts also the bond wires fatigue can accelerate the degradation of the remaining bond wires as well as the other IGBT cells under short circuits. It also shows that the IGBT cell threshold voltage degradation can lead to the specific cell that has higher short circuit current, hot spots and even thermal runaway.

Imbalanced Current and Temperature Distributions among the Parallel IGBT Chips under Short Circuit

The simulating method gives a good picture of the imbalanced current and temperature distributions among the parallel IGBT chips under short circuits. The imbalanced current/ temperature distribution is studied, and the most stressed chip is identified, which is further verified by a 1.1 kV/6 kA non-destructive tester. Both simulations and experiments show that some chips are more stressed than others during short circuits, as well as suggest a dominating effect of the inductance in the current and temperature imbalance phenomenon.

IGBT Chip Temperature during Short Circuit

Based on the proposed electro-thermal co-simulation method, the IGBT chip temperature can be beyond the rated operating temperature (typically 175 °C) with a specific 10 μs short circuit duration. However, there is still a lack of methods to directly measure the IGBT junction temperature in the time duration of several or tens of μs so far. The optical fibers and thermistor with responding time at ms-level are not fast enough. The main obstacle for infrared measurement is that black painting is required for open modules in order to achieve uniform emissivity, which also induce thermal capacitance and filter the temperature rising. While traditional temperature sensitive electrical parameters (e.g., $V_{CE,sat}$, $t_{on,delay}$) cannot be applied for abnormal conditions. A promising method can be using the short circuit itself as a TSEP, which has shown a good linearity and fast response in Chapter 5.

6.2 Research Highlights

The main contributions of this project from the author's point of view can be summarized as follows:

Physics-based Electro-thermal Simulation Tool of IGBTs under Abnormal Conditions

The proposed physics-based PSpice-Icepak co-simulation method has the capability of predicting junction temperature during abnormal operations with the consideration of: i) electro-thermal coupling effects under high current and high temperature variation conditions; ii) imbalanced current and temperature distribution inside the chip as well as the packaging during high dynamics.

A Series of Co-simulations of IGBTs Short Circuit Behavior under Different Conditions

Under new conditions, a series of electro-thermal co-simulations are performed to identify the most critical chip inside a typical MW-level IGBT power module, and the possible improvements are studied.

Under degradation conditions, a series of electro-thermal co-simulations are conducted to show the ageing effects (bond-wires lift-off, solder degradations, threshold voltage decrease) on IGBT behavior under abnormal conditions.

New 1.1 kV/6 kA Non-Destructive Tester for Short Circuit Tests

A 1.1 kV/6 kA non-destructive tester has been developed to experimentally investigate short circuit behavior of IGBT power modules. It can perform repetitive short circuit tests on IGBT modules without any damage of the device. It has been used by many research topics, for instance voltage/current oscillations study of high power modules, advanced double pulse tests (avoiding chip's self-heating effects), degradation of devices.

Comprehensive Investigations on Modern Power Devices Catastrophic Failures

A thorough investigation on catastrophic failure modes and mechanisms of modern power semiconductor devices has been addressed, including IGBTs and power diodes. Based on the catastrophic failure mechanisms, the key failure indicating parameter – the junction temperature is emphasized, which reveals the importance of thermal design and fine thermal management of IGBTs in reliability critical applications.

6.3 Proposals for Future Research Topics

Some issues of high interest for future investigations are:

Wide-Band-Gap devices short circuit behavior

Develop physics-based model for electro-thermal simulations of Wide-Band-Gap devices under abnormal conditions

Short circuit capability evaluation of wide-band-gap devices, even at high junction temperature (>200 °C)

Developing of new packages for high temperature operations (>200 °C) of wide-band-gap devices to make them more robust

Thermal imaging power devices at critical conditions

Thermal imaging wide-band-gap devices at high junction temperature operations (>200 °C)

Thermal imaging power devices before thermal runaway

Temperature evaluation of power devices under short circuits

Scale up or scale down the NDT tester for different rating power semiconductors

Alternative measurement method for junction temperature validation during abnormal conditions

Extract junction temperature of wide-band-gap devices under short circuit

Optimization of high power modules packaging from an abnormal condition point of view

Comprehensive experimental investigations on high power modules to study the parameters mismatch caused by manufacturing variations and degradations

Optimizing module layout (bus bar, geometry) to achieve better current/temperature distributions among parallel chips during abnormal situations

Design new packaging outline for high switching frequency devices

Long term reliability studies on IGBT modules

Interaction effects between abnormal operations and wear-out degradations.

Measure and model the characteristics variations due to imbalanced current/ temperature distributions among the parallel chips

Reliability evaluation and model of the repetitive short circuit ageing effects on IGBT modules

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Chapter 7

Appendix

This appendix gives the sample files for the proposed co-simulation method.

MATLAB Script Sample

```
##### Preparation State  #####
% Firstly, general settings for co-simulations
% Time step settings
NSteps = 25;    % number of steps in ICEPAK/PSPICE co-simulation
TimeStep = 1e-6;  % unit [s]  time duration of each ICEPAK/PSPICE simulation
% Geometrical constants
DicePerSide=str2double(input('Number of dice per side: ','s'));
NumberOfDice = DicePerSide ^ 2; % define number of cells in parallel in DUT chip
% Chip area ---> geometry
XDeviceSize = 0.0136;  % to be updated for different chips size
YDeviceSize = 0.0136;
DeviceArea   = XDeviceSize*YDeviceSize; % DUT chip area
ProjectName = 'Proj01'; % define project name
% Cell area ---> geometry
DeltaX = XDeviceSize / DicePerSide;
DeltaY = YDeviceSize / DicePerSide;
CellArea = DeltaX  * DeltaY;
% Secondly, settings for PSpice
%Stimula waveforms, Time-value arrays:
Von = [...
    0 0;
     4.2e-6 0;
     4.3e-6 1;
    14.3e-6 1;
    14.4e-6 0;
```

```
      80e-6 0;
      80.1e-6 0];   % short-circuit duration 4-14us
  Voff = [ Von(:,1) 1-Von(:,2) ];
% Parameters from datasheet
Rgout = 1.5;   % external gate resistance
Rcout = 2e-3; % colletor resistance
% Thirdly, settings for Icepak
% Geometry for source location
XOrigin = 0.0285; % X-Z coordinates
YOrigin = 0.0043;  % the origin is the upper-left corner
ZPlate = 0.0009; % unit [m]

##### Simulation State #####
for Step=1:NSteps,
    StartTime = (Step - 1) * TimeStep; %starting time for each step
    EndTime  =      Step * TimeStep;  %ending time for each step
    TimeNum  = EndTime * 1e6;         % number of simulation steps
   % update ANSYS new "model" file
   fID=fopen('model.template','r');  % change the model template file
    if exist('model', 'file'),
        delete('model');
    end
    foID=fopen('model','w');
   while ~feof(fID),
        % reads from the original file
        CurrentLine = fgetl(fID);
        if ~strcmp(CurrentLine, '############## SOURCE SECTION
            ##################'),
            % and writes to the new one
            fprintf(foID, '%s\r\n', CurrentLine);
        else
            % in this case, update the source sections information (e.g.,
                geometry)
            for SourceIndex = 1: NumberOfDice,
                % details omitted
            end
        end
    end
    fclose(fID);
    fclose(foID);

   % update new ANSYS "problem" file
    fID=fopen('problem.template','r'); % generate from problem template file
    foID=fopen('problem','w');
    % look for some strings in the 'problem.template' file like this one:
```

```
% ######################## array set named_point SECTION
    ########################
% and to replace them with the corresponding section:
while ~feof(fID),
    % reads from the original file
    CurrentLine = fgetl(fID);
    if strcmp(CurrentLine, '######################## array set named_point
        SECTION ######################## '),
        % in this case, put the defined source sections (e.g., geometry)
        % details omitted
        continue
    end
  % Choose if steady state ('new') or continue solution ('restart') type
    if strcmp(CurrentLine, '############### SOLVE STATEMENTS ###############'),
        fprintf(foID,['set solve_id ' ProjectName '\r\n']);
        if Step == 1,          % at the first step, start a new simulation
            fprintf(foID,['set solve_jobtype new\r\n']);
        else                        % from second step ahead, put 'restart'
            instead of 'new'
            fprintf(foID,['set solve_jobtype restart\r\n']);
        end
        continue
    end
    % Define final simulation time:
    if strcmp(CurrentLine, '############### TE STATEMENT ###############'),
        fprintf(foID,['set problem_te %4.2f \r\n'], TimeStep/1e-6); % time
            is in microseconds
        continue
    end
    % and writes to the new one
    fprintf(foID, '%s\r\n', CurrentLine);
end
fclose(fID);
fclose(foID);

%% runs the ANSYS simulation
if Step == 1,
    cd ..     %  <-------- back up to upper folder
    system(['"C:\Program Files\ANSYS
        Inc\v145\Icepak\bin\icepak14.5win64-batch.bat" -batch_solve_id '
        ProjectName ' ' ProjectName]);
  %the software installed location to be update
    cd(ProjectName);  % go to project folder (e.g. cd Proj01)
% from the second step, data exchange between ANSYS and PSpice
else
```

```
    % in further steps, it runs batch file
    % prepare the executing file (.uns_in file) for FLUENT
    fiID=fopen('PROJxx.uns_in.template','r'); % opens the template
    foID=fopen([ProjectName '.uns_in'],'w');
    % replace each string like this one:
    % #####PROJNAME#####
    % with the ProjectName variable
  % details omitted
    fclose(fiID);
    fclose(foID);
    % prepare the batch file:
    fiID=fopen('PROJxx_scr.bat.template','r'); % opens the template
    foID=fopen([ProjectName '_scr.bat'],'w');
    % replace each string like this one:
    % #####PROJNAME#####
    % with the ProjectName variable
  % details omitted
    fclose(fiID);
    fclose(foID);
% update the power loss information based on PSpice results:
 fiID=fopen('Projxx.udf.c.template','r'); % opens the template
    foID=fopen([ProjectName '.udf.c'],'w');
    % details omitted
    fclose(fiID);
    fclose(foID);
 % run the batch file:
    system([ProjectName '_scr.bat']);
 end

%% Pspice section
 % creat the .cir file based on template
 fID=fopen('Stepxx.template','r');
 foID=fopen(['Step' sprintf('%03d', Step) '.cir'],'w');
 % omitted
 while ~feof(fID),
    % reads from the original file
    CurrentLine = fgetl(fID);
    % define stimulating profile in 'Variable generators' section,
    if strcmp(CurrentLine, '##################### VARIABLE GENERATORS
        ########################'),
       % details omitted
       continue % stops and skip to the next template line
    end
    % define IGBT cells in the 'IGBT GENERATOR' section,
       if strcmp(CurrentLine, '##################### IGBT GENERATORS
```

```
                ########################'),
                % details omitted
                continue % stops and skip to the next template line
            end
        % define energy monitoring nodes in the 'ENERGYNODE STATEMENTS' section,
            if strcmp(CurrentLine, '############ ENERGYNODE STATEMENTS
                ##############'),
               % details omitted
             continue % stops and skip to the next template line
            end
        % define simulation conditions in the 'Simulation statements' section,
        if strcmp(CurrentLine, '############ SIMULATION STATEMENTS
             ##############'),
            % details omitted
            continue % stops and skip to the next template line
        end
        % if no matches, it writes straight to the .CIR file
        fprintf(foID, '%s\r\n', CurrentLine);
    end
    fclose(fID);
    fclose(foID);
   % create the Pspice command file:
       CmdFID=fopen('mybatch.txt','w');
       % details omitted
       fclose(CmdFID);
       !type mybatch.txt
    fprintf('\n\nSpice is running\n\n');
    % Run PSPICE directly
    !"C:\Cadence\SPB_16.3\tools\pspice\pspice.exe" -c mybatch.txt
    %read PSPICE output results
    fResID=fopen(['Step' sprintf('%03d', Step) '.out']);
    % details omitted
    fclose(fResID);
    fprintf('\n');
end
```

PSpice Circuit Template Sample

```
STEPxx.CIR - multiple cells PSPICE
.options vntol=1e-6 itl4=100 itl1=2000 itl2=2000
.options reltol=0.01 abstol=1e-9
* dummies
L  L  C1 38nH ; test circuit stray inductance
Cl L  C1 100pF
```

```
.lib igbt1700_Ver03.lib
* generators changing with time
#################### VARIABLE GENERATORS ########################
* diode model
.model dfast D(Is=1.e-16 Cjo=400p Tt=10n);
.model dideal D(Is=1.e-16);
* Switch model
.model Sbreak VSWITCH Roff=1e6 Ron=1ohm Voff=0.0 Von=1.0 ;
* IGBT
#################### IGBT GENERATORS ########################
*X001 C0010 G0010  0 T DUT PARAMS: CELL_AREA =1.188100e+00
Rex  Gex1 G1 20
Sa Gex1 13 100 0 Sbreak
Sb Gex1 15 200 0 Sbreak
Ron   13 14  15      ;turn-on resistance
Roff  15 16  60      ;turn-off resistance
V1 14  0  15V
* Absolute clock
Cclock 100T 0   1uF
Rclock 100T 0   1Meg
Iclock 0   100T 1A  ; 1V/us at node 100T absolute time
############ ENERGYNODE STATEMENTS #############
*.print TRAN V(100E) ;energy node -> results in the output file
############ SIMULATION STATEMENTS #############
* .tran (5us 5us 0us 5ns) UIC ; the UIC option must be included starting from
    2nd step
* .savebias "status02.sav" TRAN TIME=1u ; the filename must be changed
* .inc "status01.sav"          ; the .inc must be included starting from 2nd
    step
.probe
.end
```

ANSYS Files Sample "model" file:

```
# Icepak 14.5.2 model file
......
object block IGBT2_Region1
       thermal_heat_tr_face_profile {-28.4715 -4.2957 -0.72927}
       current_stype hexa
       block_type solid
       obj_color_default 0
       solid_material Si
       shape body_shape shape_hexa
           config -grid_length {0 0 0} -grid_height {0 0 0 0 0 0 0} -grid_ratio
```

```
            {0 0 0 0 0 0 0}
        setval point1 {0.02850000000000108 0.004299999999999749
            0.0007300000000000084} point2 {0.04209999999999781
            0.01790000000000092 0.0009200000000000319} diff
            {0.01359999999999673 0.01360000000000117 0.0001900000000000235}
            volume_flag {1} diff_flag {0}
        setunits ys mm ye mm xs mm zs mm xe mm ze mm
    end shape
    grid_priority 20
    creation_order 40
    current_genus default
    obj_color #ff00ff
    mlm_level 0
  end object
%set the source information
############## SOURCE SECTION ##################
......
```

"problem" file:

```
# Icepak 14.5.2 model file
......
set problem_ts 0
%set the simulation ending time
############## TE STATEMENT ##############
set problem_temp 20
set problem_pressure 0
......
set solve_remote {}
%set the simulation type new or restart
############## SOLVE STATEMENTS ##############
set solve_jobinterp {}
%set the monitoring point information
######################### array set named_point SECTION ######################
......
```

Journal Papers

Publication 1

(*Journal Paper*)

Overview of Catastrophic Failures of Freewheeling Diodes in Power Electronic Circuits

Wu, Rui; Blaabjerg, Frede; Wang, Huai; Liserre, Marco

The paper has been published in the
Microelectronics Reliability, vol. 59, no. 9-11, pp. 1788–1792, Sept. 2013.

DOI:10.1016/j.microrel.2013.07.126

Microelectronics Reliability 53 (2013) 1788–1792

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Overview of catastrophic failures of freewheeling diodes in power electronic circuits

R. Wu *, F. Blaabjerg, H. Wang, M. Liserre

Centre of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Pontoppidanstraede 101, 9220 Aalborg, Denmark

ARTICLE INFO

Article history:
Received 24 May 2013
Received in revised form 14 July 2013
Accepted 20 July 2013
Available online 23 August 2013

ABSTRACT

Emerging applications (e.g. electric vehicles, renewable energy systems, more electric aircrafts, etc.) have brought more stringent reliability constrains into power electronic products because of safety requirements and maintenance cost issues. To improve the reliability of power electronics, better understanding of failure modes and failure mechanisms of reliability–critical components in power electronic circuits are needed. Many efforts have been devoted to the reduction of IGBT failures, while the study on the failures of freewheeling diodes is less impressive. It is of importance to investigate the catastrophic failures of freewheeling diodes as they could induce the malfunction of other components and eventually the whole power electronic circuits. This paper presents an overview of those catastrophic failures and gives examples of the corresponding consequences to the circuits.

1. Introduction

Power electronics plays an important role in energy conversion applications, such as motor drives, utility interfaces with renewable energy sources, power transmission (e.g. high voltage direct current systems, and flexible alternating current transmission systems), electric or hybrid electric vehicles. Therefore, the reliability of power electronics becomes more and more vital, and should draw more attention [1]. According to a survey, semiconductor failures and soldering joints failures in power devices take up 34% of power electronic system failures [2]. Another survey shows that around 38% of faults in variable speed ac drives are due to failures of power semiconductor devices [3]. A recent questionnaire on industrial power electronic systems also shows that the responders regard power electronic reliability as an important issue, and 31% of responders selected power semiconductor devices as the most fragile component in their applications [4]. Therefore, it demands a better understanding of failure mechanisms of power semiconductor devices so as to reduce their failure rates.

Diodes and Insulated Gate Bipolar Transistors (IGBTs) are two kinds of reliability–critical power semiconductor devices widely used in power electronic circuits [1]. Power diodes are usually assumed to have outstanding ruggedness performance. However, freewheeling diodes fail under various circumstances, especially during the turn-on transition of IGBTs in high switching frequency applications. The freewheeling diodes slow down the switching speed of the IGBTs due to severe stresses induced by the reverse recovery process. Therefore, it is worth to investigate the failures of freewheeling diodes and exploring the solutions to improve the reliability of both freewheeling diodes and IGBTs.

Diode failures can generally be classified as catastrophic failures and wear out failures. Diode wear out failures are mainly induced by accumulated degradation with time, while catastrophic failures are triggered by single-event overstress, such as overvoltage, overcurrent, overheat. Prognostics and Health Management (PHM) method can monitor the degradation of diodes and estimate wear out failures [5]. However, PHM is not applicable for catastrophic failures, which are more difficult to be predicted.

Several overview papers cover the topic on diode failures. In [6], Rahimo et al. discuss the major reverse recovery failure modes of freewheeling diode in IGBT applications. While it only focuses on snappy recovery and dynamic avalanching, no static failure is mentioned. In [7], Ciappa gives a comprehensive overview on the wear out failure mechanisms of power semiconductor devices, such as bond wire fatigue, aluminum reconstruction, substrate cracking, interconnections corrosion, and solder fatigue and voids. However it mainly focuses on IGBT, and freewheeling diodes catastrophic failures are not discussed. Therefore, a detailed and comprehensive review on diode catastrophic failures is still lack in the prior-art literatures. Moreover, it is also worth to investigate the influence of freewheeling diode failures to IGBT operations in power electronic converters.

The aim of this paper is to provide a review of the key behaviors of diode catastrophic failure due to overstresses and the corresponding influence to IGBTs in power electronic circuits. Section 2 classifies the types of freewheeling diode catastrophic failures. Section 3 summarizes the catastrophic failures of diode in terms of failure mode and failure mechanism. Section 4 investigates the influence of freewheeling diode failures to IGBT operations in

* Corresponding author. Tel.: +45 2963 2067; fax: +45 9815 1411.
E-mail address: rwu@et.aau.dk (R. Wu).

0026-2714/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.microrel.2013.07.126

power electronic converters, followed by the conclusion in Section 5.

2. Classification of failure modes of freewheeling diodes

The catastrophic failure modes of freewheeling diodes can be classified into open-circuit failures and short-circuit failures. Normally open-circuit failures are considered not fatal to converters, since the converter can operate with lower quality of output [8]. On the contrary, short-circuit failures are more fatal to converters, as the uncontrolled short-circuit current may destroy the active switching devices (e.g. IGBTs) or other components in the circuit. Fig. 1 shows the typical open-circuit failures and short-circuit failures of freewheeling diodes.

2.1. Open-circuit failures

Freewheeling diode open-circuit failures are generally due to mechanical causes. Open-circuit failure mode can happen because of external disconnections due to vibration, or internally by bond wire lift-off or rupture after temperature swings or high short-circuit current.

2.2. Short-circuit failures

Short-circuit is also a common failure mode of freewheeling diodes in power electronic circuits. Failures can happen during reverse blocking state as well as the reverse recovery transition. Fig. 2 shows the definition of reverse and forward voltage for diodes [9]. There are five major failure mechanisms as shown in Fig. 1, which will be discussed in next section.

3. Major failure mechanisms of freewheeling diodes

3.1. Open-circuit mechanisms

Similar to IGBTs, diode open-circuit will not be initially fatal to the converter, but may result in secondary failures of other devices in a power electronic circuit due to interaction among them.

The mechanism is similar to that of IGBTs. Bond wire lift-off failure can happen after short-circuit, caused by high temperature fatigue and the mismatch of Coefficients of Thermal Expansion (CTEs) between Silicon and Aluminum. Crack may also be initiated at the periphery of the bonding interface, and the bond wire finally lifts-off when crack propagates to the weaker central bonding area. Central bond wires normally fail at first, and then the survivor bond wires follow [10]. Bond wire rupture is usually slower than lift-off mechanism and usually observed after long power cycling tests or long time operation.

3.2. Short-circuit mechanisms

The short-circuit failures of freewheeling diode could lead to potential destruction to the relevant IGBTs, and other components, as it induces uncontrolled high current to the circuit. The failure

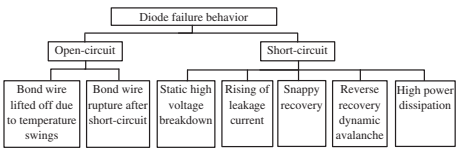

Fig. 1. Overview of freewheeling diodes catastrophic failures.

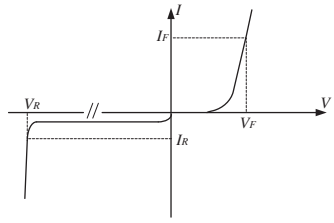

Fig. 2. Definition of reverse and forward voltage of diodes.

mechanisms can be static high voltage breakdown, leakage current rising, snappy recovery, dynamic avalanche during reverse recovery, as well as high temperature due to the power dissipation and so on.

3.2.1. Static high voltage breakdown

High reverse voltage can cause diodes static avalanche. With reverse voltage reaching first static avalanche point, the current rises with positive slope, while no permanent failure happens. If the voltage reaches the second avalanche point, there will be a Negative Differential Resistance (NDR), which will lead to the current filament and a quick short-circuit. Detailed numerical simulations are carried for a rated 3.3 kV/1 kA diode, and the results are shown in Fig. 3 [11]. Another research reveals metallization between copper and silicon can also lead to diode electrical breakdown [12]. It is also revealed that the avalanche capability is strongly dependent on the initial breakdown location and the edge termination design by numerical simulation and experiments, and the common failure locations are near the chip's edge and the bond wires [13]. Since operating voltage of freewheeling diodes is normally much lower than rated voltage, static high voltage breakdown is not common in nowadays applications.

3.2.2. Rising of leakage current

The leakage current of power diodes is usually very low, but it increases with voltage and temperature. The value is roughly doubled for every 10 °C raise of temperature. This effect is more obvious for gold-diffusion diodes, which may be thermally destroyed at high temperature [9].

With operating voltage and temperature above the rating parameters, leakage current increases dramatically and the diodes fail into short circuit at the chip's peripheral surface [14,15]. Experiments show that the diodes operation temperature can be increased without risks of failure by improving the junction edge current control, like a junction passivation process [16,17]. A further research reveals the mechanism is junction carrier avalanche multiplication, and the weak spots are near the chips' edge [18]. The leakage current rising can also be due to repetitive electrostatic discharge [19]. Since short-circuit failures during freewheeling diode reverse status can damage IGBT and circuit quickly, it is critical to prevent this event.

3.2.3. Snappy recovery

Freewheeling diodes are prone to fail easily during reverse recovery process because of snappy recovery. The behavior of snappy recovery is shown in Fig. 4, in which a steep decline in the current is observed after the reverse recovery current reaches the peak value. The main reason is the sudden disappearance of the remaining carriers at the end of the recovery process. Due to high *di/dt* and stray inductance in the circuit, high voltage spikes can appear and damage the diode.

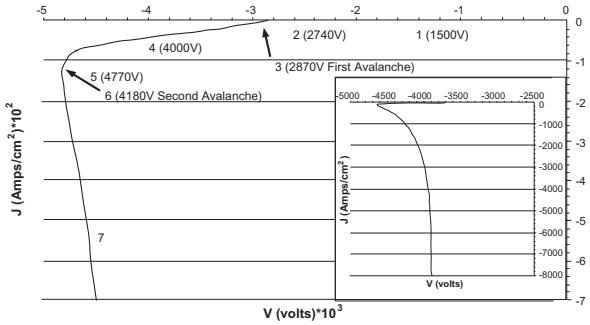

Fig. 3. First and second static avalanche breakdown of a 1700 V rated power diode [11].

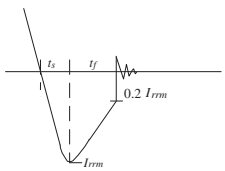

Fig. 4. Current characteristics of snappy reverse recovery behavior [9].

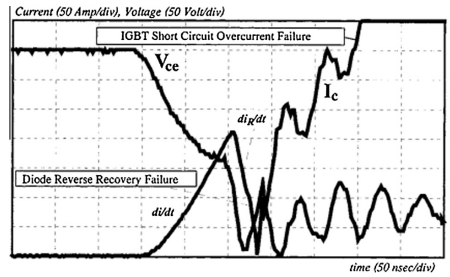

Fig. 5. Freewheeling diode reverse-recovery failure with IGBT short circuit failure [6].

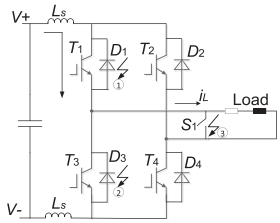

Fig. 6. Operation of a single phase inverter under different failure conditions – ① reverse recovery transition, ② reverse state, ③ load short-circuit.

It has been validated that both reverse recovery charge and time increase with diode effective contact area, and snappy recovery is clearly observed for larger area in numerical simulation and experiments [20]. Thus special attention should be paid to choose the diode size for avoiding diode failures. H+ irradiation has been proposed to obtain trade-off between diodes switching speed and softness, which can avoid snappy recovery, validated by comprehensive experiments and numerical investigations [21–23]. A new design procedure of freewheeling diodes based on measurement and simulation is also proposed to improve the reverse recovery softness [24]. Controlled Injection of Backside Holes (CIBH) diodes are also proposed to increase the soft reverse recovery behavior [25]. However, it is still a critical point to avoid snappy recovery when designing freewheeling diodes.

3.2.4. Reverse recovery dynamic avalanche

Dynamic avalanching occurs at high di/dt switching speeds, as shown in Fig. 5. Dynamic avalanching can result in the generation of a hot spot in the silicon die itself due to non-uniform current crowding which leads to the destruction of the device. The causes of these hot spots can range from process to material variations in a single diode silicon chip [26].

Impact ionization near N-N+ junction is considered as the main reason for the failure. It leads to the negative differential resistance and current filament, finally a thermal runaway [27–30]. This process called Egawa effect [26] is very similar to the second breakdown in bipolar transistors. Local heating and explosion at the corner of anode is observed even the reverse voltage is lower than static breakdown voltage [31]. A detailed study of dynamical behavior of the plasma layer also explains this reverse recovery failure [32,33]. To avoid the second current bump observed during reverse recovery failure, a merged P-i-N Schottky diode is proposed to replace conventional P-i-N freewheeling diode [34]. It shows deep N+ emitter and wide n-base can improve the dynamic avalanche characteristic in 2*D* simulations [35,36]. It is also proved CIBH diode can prevent the filaments in N-N+ junction by 2D numerical simulations [33]. An improved impact-ionization model is proposed to simulate high electrical fields in diodes [37]. Electro thermal simulations show that thermal-induced filament can lead to destructive thermal runway and it is sensitive to contacts thermal resistance [38]. There could be further work to improve both die structure and thermal performance.

3.2.5. High power dissipation

When the diode forward current is high and temperature is rising, the forward voltage will increase. If the forward voltage

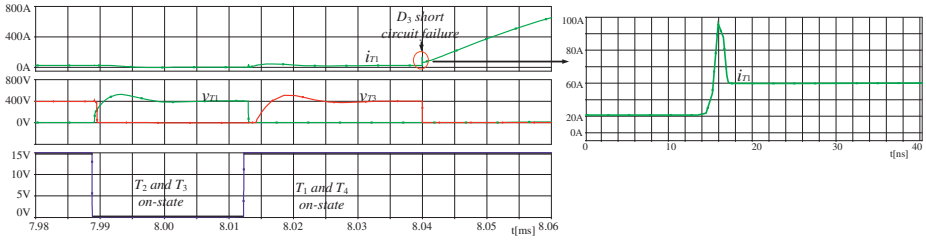

Fig. 7. PSpice simulation waveforms of IGBTs after D_3 short circuit in reverse state.

exceeds a specified limit value, the overload high power dissipation may fatally damage the silicon die [9].

4. Influence of freewheeling diode failures on the operations of IGBTs in power electronic circuits

Fig. 6 shows a single phase inverter consisting of IGBTs (T_1–T_4) diodes (D_1–D_4), and stray inductance L_s (which may lead vital stress to device).

The operation of the inverter is as follows: initially, T_2 and T_3 are on, the current i_L flows through the load, then T_2 and T_3 are turned-off and T_1 and T_4 are switched on after a certain period of dead time. Because the load determines the direction of the current flow, the current will flow through the diodes D_1 and D_4 back to the voltage source. After i_L decreases to zero and to the negative, the current will flow through T_1 and T_4.

There are three typical failure behaviors:

(a) When the current is commutating from diode to IGBT, the freewheeling diode reverse recovery failure may lead to an IGBT short-circuit failure, as shown by ① in Fig. 6.
(b) When IGBTs T_1 and T_4 are on, and the current i_L flows through the load, reverse diode D_3 fails into the short-circuit, the short-circuit current between $V+$ and $V-$ may damage T_1 fast, as shown ② in Fig. 6.
(c) When current is flowing through D_1 and D_4, a load short circuit will cause overstress of the diodes and IGBTs (symbolized as ③ – closing the switch S_1 in Fig. 6). As the current flowing through D_1 and D_4 will be commutated to T_1 and T_4 rapidly, short-circuit current on IGBTs will be larger. During the transient, both the high reverse recovery current and the voltage may produce large energy dissipation and damage the diode. However, the IGBT may also fail first if the peak voltage is over the rated voltage [39].

As an example, Fig. 7 shows the simulation results of the scenario ② in which D_3 is short during the conduction of T_1. It could subsequently induce the failure of T_1 due to its increased current stress as shown in Fig. 7.

5. Conclusions

The typical failure modes and failure mechanisms of freewheeling diodes due to over stresses are overviewed in this paper. Initial short-circuit failures may lead to open-circuit finally. Short-circuit failures can happen at five typical occasions.

The influence of the freewheeling diode failures to IGBT failures is also investigated on the circuit level. The associated behaviors of the IGBTs are also briefly described.

The overview in this paper could be useful for further work in the following areas: correlations between IGBT and diode failures; improvements of diode performance due to failure mechanisms; effective protection circuits dealing with different catastrophic failures; fault tolerant design coping with freewheeling diode catastrophic failures; better models of failure mechanisms; better models and tests of devices beyond the specific rating.

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Publication 2

(*Journal Paper*)

Study on Oscillations during Short Circuit of MW-Scale IGBT Power Modules by Means of a 6-kA/1.1-kV Nondestructive Testing System

Wu, Rui; Reigosa, Paula Diaz; Iannuzzo, Francesco; Smirnova, Liudmila; Wang, Huai; Blaabjerg, Frede

The paper has been published in the
IEEE Journal of Emerging and Selected Topics in Power Electronics,
vol. 3, no. 3, pp. 756-765, Sept. 2013.

DOI:http://dx.doi.org/10.1109/JESTPE.2015.2414448

Study on Oscillations During Short Circuit of MW-Scale IGBT Power Modules by Means of a 6-kA/1.1-kV Nondestructive Testing System

Rui Wu, *Student Member, IEEE*, Paula Diaz Reigosa, *Student Member, IEEE*, Francesco Iannuzzo, *Senior Member, IEEE*, Liudmila Smirnova, *Student Member, IEEE*, Huai Wang, *Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*— This paper uses a 6-kA/1.1-kV nondestructive testing system for the analysis of the short-circuit behavior of insulated-gate bipolar transistor (IGBT) power modules. A field-programmable gate array enables the definition of control signals to an accuracy of 10 ns. Multiple 1.7-kV/1-kA IGBT power modules displayed severe divergent oscillations, which were subsequently characterized. Experimental tests indicate that nonnegligible circuit stray inductance plays an important role in the divergent oscillations. In addition, the temperature dependence of the transconductance is proposed as an important element in triggering for the oscillations.**

***Index Terms*— Insulated-gate bipolar transistor (IGBT), nondestructive testing, oscillations, power modules, reliability, short circuit.**

I. Introduction

MODERN power electronics systems face increasing demands to improve entire system endurance and safety while reducing manufacturing and maintenance costs [1], [2]. When questioned, manufacturers place semiconductor devices as the most critical and fragile component in industrial power electronic systems [3]. In [4], semiconductor failure and solder joint failure in power devices accounted for 34% of power electronic system failures. Because insulated-gate bipolar transistors (IGBTs) are the most widely used power semiconductor device in industrial power electronic systems in the range above 1 kV and several tens of kilowatts, the reliability of IGBTs has been drawn significant attention. Due to the ease of maintenance at affordable cost [5], power modules are the most used package in medium and high-power applications. An IGBT's ability to withstanding abnormal conditions (e.g., short circuits or overloads) is a particular requirement for adequate robustness in various applications [5]–[7].

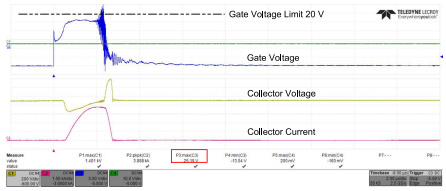

Fig. 1. Evidence of oscillations occurring during a short-circuit test of a 1.7-kV/1-kA IGBT power module performed at 900 V of collector voltage. Time scale: 2 μs/div. Gate voltage: 5 V/div. Collector voltage: 200 V/div. Collector current: 1 kA/div. The gate peak voltage was 25.19 V, whereas the absolute maximum rating for this device is $\pm$20 V.

Recently, the paradigm shift from classical handbook-based methods to physics-of-failure approach is discussed to identify the failure mechanisms of critical components in power electronic systems. This approach is a methodology based on a comprehensive root-cause analysis, including the impact of material defects and stressors on power electronics devices, which will drive the multidisciplinary research on reliability in the next decades [8]. The wearout mechanisms of IGBT modules due to long-term degradation are well studied in the last two decades [9], [10]. Some of the catastrophic failure mechanisms due to single-event overstresses are also discussed in [11]. Meanwhile, it is a hot research topic to study some experimentally observed failure during short circuits within the allowable operation time (e.g., 10 μs). For example, short circuits can destroy devices through thermal runaway or initiate uncontrolled divergent oscillations [12], which, in turn, can dramatically lead to the device destruction in a few microseconds. Fig. 1 displays an example of such

Manuscript received November 3, 2014; revised February 2, 2015; accepted March 4, 2015. Date of publication March 20, 2015; date of current version July 30, 2015. This work was supported by the Center of Reliable Power Electronics Project framework through Aalborg University, Aalborg 9100, Denmark. Recommended for publication by Associate Editor A. K. Rathore.

R. Wu, P. Diaz Reigosa, H. Wang, and F. Blaabjerg are with the Centre of Reliable Power Electronics, Aalborg University, Aalborg 9100, Denmark (e-mail: rwu@et.aau.dk; pdr@et.aau.dk; hwa@et.aau.dk; fbl@et.aau.dk).

F. Iannuzzo is with the Centre of Reliable Power Electronics, Aalborg University, Aalborg 9100, Denmark, and also with the Department of Electronic and Information Engineering, University of Cassino and Southern Lazio, Cassino 03043, Italy (e-mail: fia@et.aau.dk).

L. Smirnova is with the Department of Electrical Engineering, Lappeenranta University of Technology, Lappeenranta 53850, Finland (e-mail: lyudmila.smirnova@lut.fi).

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Digital Object Identifier 10.1109/JESTPE.2015.2414448

oscillations from a commercial 1.7-kV/1-kA IGBT power module. The short-circuit duration, shown in Fig. 1, is far below the demands of many IGBT application engineers, which is traditionally $\sim$10 μs.

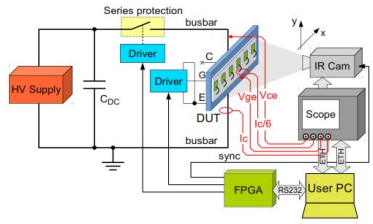
Furthermore, IGBT manufacturers continuously develop new generation devices with faster commutation speeds in order to reduce the switching losses. The faster switching speed requires higher transconductance (i.e., the output current driven at a given gate voltage) and a consequent higher amplification gain for a given chip area. This improvement can lead to instabilities during short circuit, where both high current and voltage are applied at the same time. In new generation IGBTs, the amplification gain can be so high that may introduce possible diverging oscillations [12], which can damage the device in a few microseconds as soon as the gate voltage amplitude reaches the oxide breakdown voltage.

Even so, much research in the past has focused on the short-circuit behavior of IGBT power modules. In [13], short-circuit capability was studied by repetitive low-energy-level short-circuit tests, and revealed that the short-circuit current reduced throughout the test due to aluminum degradation and the consequent increase in the ON-state resistance. In [14], the statistical distribution of the short-circuit peak current among IGBT modules from a production lot was investigated. In the same investigation, an electrothermal model based on a physical approach was developed to simulate the current distribution and the thermal imbalance among the IGBT chips inside power modules. In [15], extensive 2-D numerical simulations were performed to analyze and improve the short-circuit performance of 3.3-kV field-stop (FS) technology clustered IGBT. In [16], short-circuit tests were applied to 1200 V Si trench-gate FS IGBTs up to 200 °C. Finally, gate voltage oscillations have been experimentally observed during ON-state short circuits for both IGBTs housed in both traditional power modules and press-pack packaging [17], [18]. In spite of the previous work, the instability evidenced in Fig. 1 still lacks of interpretation as it takes place during the turn OFF phase.

Recently, several nondestructive testing concepts have been proposed to perform repetitive overcurrent and short-circuit testing of IGBTs while avoiding significant device damage. The implementation of nondestructive testing systems for discrete IGBTs (up to 100 A) and for higher power IGBT modules (up to 2.4 kA) was discussed in [19] and [20]. The main focus is to study IGBT short-circuit behavior at various electrical conditions.

In this paper, the short-circuit study of high-power IGBT modules is performed on a state-of-the-art nondestructive tester (NDT) with current and voltage limits of 6 kA and 1.1 kV. A comprehensive investigation of the short-circuit behavior of megawatt-scale IGBT power modules has been conducted, with particular focus on oscillations occurring during short-circuit turn OFF.

This paper is organized as follows. Section II describes the principle of the NDT, including the circuit structure, low inductance busbar, and field-programmable gate array (FPGA)-based supervising unit. Section III presents experimental short-circuit results, including oscillation dependence on collector voltage. Section IV is a discussion about the mechanisms causing the oscillations. Finally, the conclusion is drawn in Section V.



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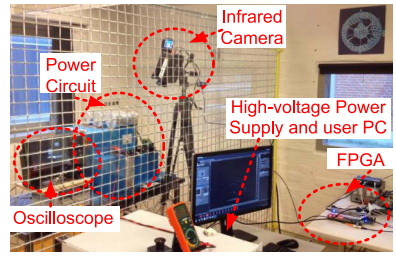


(b)

Fig. 2. (a) Principle schematic of the proposed NDT. (b) Picture of the laboratory setup.

II. Description of the Nondestructive Testing System

A. Structure and Operating Principle

The basic principle of the nondestructive testing technique is to perform repetitive tests up to the physical limits of the device under test (DUT) while avoiding device destructions. This characteristic is particularly desirable as it permits post-failure analyses in case of device rupture. At the same time, the technique presents challenges due to requiring one or more additional protection switches, typically set in series to the DUT. These have higher nominal voltage and current ratings and should not alter the overall circuit inductance significantly. Fig. 2(a) shows the principle schematic of the proposed NDT. The NDT structure is described as follows. A high-voltage power supply charges up preliminarily a capacitor bank C_{dc} to a specific testing voltage. This capacitor bank supplies all the energy required for the test. A series protection switch is connected between the capacitor bank and the DUT. It is turned ON before the short circuit is made and switched OFF right after the test in order to save the DUT from possible explosions. As discussed above, the rating of the series protection switch is larger than the DUT, which can cause a large increase in the overall stray inductance. However, careful consideration was made in the design of the busbar [21], [22]

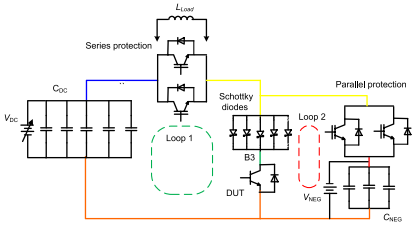


Fig. 3. Detailed schematic of the nondestructive testing circuit.

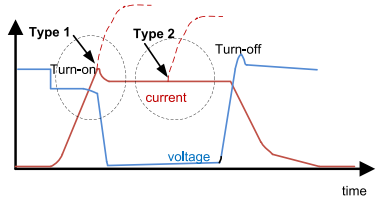


Fig. 4. Two possible types of short circuits. The Type 1 occurs during turn ON, whereas the Type 2 occurs during the conduction state.

TABLE I
RATINGS OF THE MAIN COMPONENTS IN THE CIRCUIT IN FIG. 3

Characteristic	Value
DC Maximum voltage	1.1 kV
DUT Maximum current	6 kA
DC capacitors C_{DC}	5 x 1100 μF, 1100 V
Stray inductance of the main loop	37 nH
Series protection	2 x Dynex DIM1500ESM33-TS000 3 kA/ 3.3 kV
Parallel protection	2 x Mitsubishi CM1200HC-66H 2.4 kA/ 3.3 kV
Auxiliary capacitors C_{NEG}	3 x 1100 μF, 1100 V
Schottky diodes	5 x 170 V, 1.2 kA

and an optimized busbar was developed to minimize the overall circuit inductance. The overall circuit inductance is calculated through the use of a commercial computer-aided design tool (CAD tool) and a finite-element method (FEM) software (Ansys Q3D) [23], [24]. In case an open DUT is available, an infrared camera FLIR X8400sc [25] can also be used to obtain the temperature distribution among the internal chips. A supervising unit, based on the Altera Cyclone IV FPGA, is used to provide the driving signals for the DUT, the protection switch, and the infrared camera. It also provides the precise time control for electrical measurement with an accuracy of 10 ns. A LeCroy HDO6054-MS oscilloscope is used for the acquisition of the waveforms. A personal computer (PC) is the user interface, which is connected to the equipment via an Ethernet link and an RS-232 bus. Two commercial IGBT drivers drive the protection switches and the DUT. To perform short circuits, the protection circuit on the DUT drivers is deactivated. During each short circuit, the collector current, collector voltage, and gate voltage waveforms are acquired. Fig. 2(b) shows a photograph of the laboratory setup, which is behind a safety cage, together with the PC and FPGA board. Behind the cage, the power circuit can be identified together with the oscilloscope and the infrared camera.

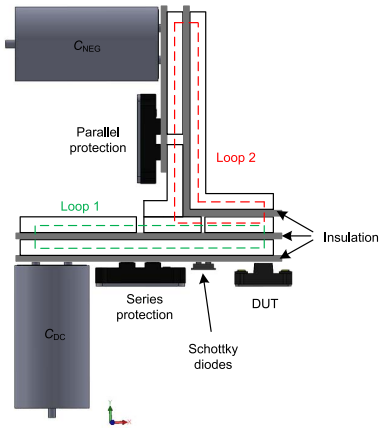
A detailed electrical schematic of the NDT is shown in Fig. 3. Table I summarizes the specifications of the components. There are several components in parallel to enlarge the current capability and to minimize the stray inductance at the same time. The main difference with respect to Fig. 2(a) is the presence of an additional leg in parallel to the DUT, where a parallel protection is included together with a capacitor bank C_{NEG} and a battery V_{NEG}. In the same schematic, five Schottky diodes and an optional load inductance L_{Load} are included too. The circuit is divided into two loops: 1) Loop 1 is the main loop, including the series protection; and 2) Loop 2 includes the parallel protection. The DUT is located in the common branch. The parallel protection has a twofold role: 1) to assist the series protection during its turn OFF by diverting the typical tail current of IGBTs; and 2) to act as a crowbar in case that any instability happen. To enhance its promptness and effectiveness, a negative bias is fed to its emitters by the battery V_{NEG} and the capacitors C_{NEG}. In this way, the typical large voltage tail at the turn ON of the IGBT switches is accelerated and the voltage zeroes more promptly. To prevent supplying negative voltage to the DUT, Schottky diodes are placed in the circuit.

An optional inductance L_{Load} can be placed to perform different types of short circuit. As shown in Fig. 4, there are mainly two different types of short circuit: 1) a Type 1 short circuit happens during the DUT turn ON; and 2) a Type 2 short circuit happens during the DUT ON-state. The NDT can provide both short circuit types by different configuration and control timing schemes. In case of Type 2 short circuit, the inductance L_{Load} is used to simulate the load. The control time schemes for the two types will be illustrated in Section II-C.

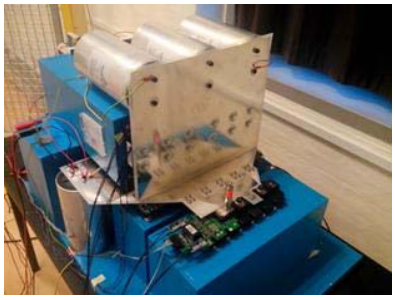
B. Low Inductance Busbar

The high current slope during turn ON and turn OFF under short circuits (i.e., at kiloampere per microseconds level) necessitates that stray inductance is kept to a minimum. The busbar design of the NDT power circuit is shown in Fig. 5(a) and (b). Fig. 5(a) provides a cross section of the NDT: 1) the DUT is the black module in the lower right corner; and 2) the two capacitor arrays C_{dc} ($5\times$) and C_{NEG} ($3\times$) are located under and behind the busbars, respectively. The series and parallel protection are also located under and behind the busbars, respectively. The Schottky diodes are installed in five square windows close to the DUT. The adopted T-shaped geometry allows observing the DUT's temperature distribution from the top with the infrared camera.

A Mylar isolation foil has been used for the busbar. The design of the geometry has been performed with a 3-D CAD tool in order to optimize the placement of the



(a)



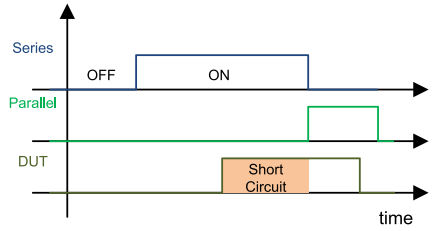
(b)

Fig. 5. Busbar design of the nondestructive testing circuit. (a) Principle cross section of the busbar layers using the same layer colors in Fig. 3. Loop 1 is the horizontal one. Loop 2 is the vertical one. (b) Picture of the physical prototype.

components in a way that mutual coupling among them reduces the overall inductance value. Ansys Q3D was used to repeatedly verify such placement until the best configuration was achieved. The low stray-inductance design has been verified by experimental tests in Loop 1 with a result of 37 nH, including the intrinsic inductances of the series protection and the capacitors. This value is even lower than theoretical calculations [24]. Fig. 5(b) shows the whole assembly design and the relative picture.

C. FPGA-Based Supervising Unit

As discussed in Section II-A, short circuits can be classified as Type 1 and Type 2. Type 1 happens at the device turn ON. In this case, there is no need for the load inductance L_{Load}, hence it is removed from the circuit. As shown in Fig. 6(a), the series protection is preliminarily turned ON and the parallel



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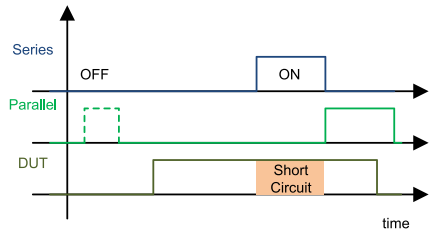
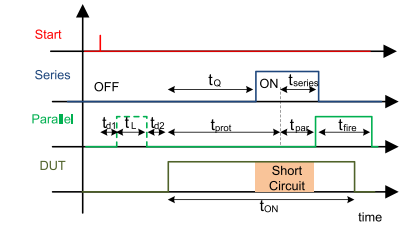


(b)

Fig. 6. Timing settings for two types of short circuits. (a) Timing diagram for Type 1 short circuit. (b) Timing diagram for Type 2 short circuit.

protection is turned OFF. Since Schottky diodes behave almost like ideal diodes, the DUT works as if it were connected directly to the C_{dc} capacitors. The DUT is then turned ON, and a short circuit occurs [shadowed period in Fig. 6(a)]. After a given delay, the series protection is switched OFF and the parallel protection is switched ON, and the short-circuit waveforms are acquired from the DUT turn ON until the firing of the protection. Several tests are performed step-by-step at increasing delays, up to the programmed DUT on time. In this way, if any instability begins to occur at a specific step, the sequence is stopped and damage to the DUT can be avoided.

Contrarily to Type 1, a Type 2 short circuit happens during the ON-state of the device. In this case, the inductance, L_{load}, is required to simulate the load. Referring to Fig. 6(b), the parallel protection is turned ON first, while the series protection is still OFF. This preliminary phase is very similar to the double pulse test concept, where a first pulse is used to magnetize the load inductance [26]. However, contrary to double pulse tests where the DUT itself is used to such an aim, here the parallel protection is used instead, so any possible self-heating on the DUT is avoided. This can guarantee that tests are performed at stable temperatures in the DUT. The series protection's diodes operate as freewheeling diodes for the load inductance. Then, the DUT is turned ON and a normal commutation happens. After that, the series protection is switched ON and a short circuit is induced. After a specified delay, the series protection is switched OFF and the parallel protection is switched ON. Similarly to the Type 1 short circuit, several tests are performed step-by-step at increasing delays, up to the programmed DUT conduction time.



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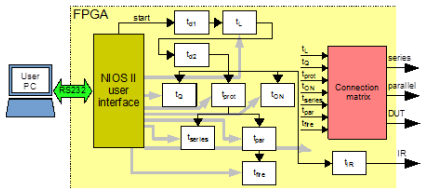


(b)

Fig. 7. FPGA supervising unit. (a) Operation timings. (b) Implementation schematic. The NIOS II user interface provides the delays to the several timers of the circuit (gray arrows) and the start signal that initiates the timing sequence.

The above time sequences are generated by an FPGA-based supervising unit, as shown in Fig. 7(a). It can be recognized that the sequences shown in Fig. 6(a) and (b) can be obtained by a proper choice of the times shown in Fig. 7(a). Moreover, when the infrared camera is used, an additional signal is generated synchronously with the DUT signal at increasing delays. This latter feature is required to obtain a stroboscopic infrared acquisition during the test. A development board DE2-115 from Terasic Corp [27] hosting an Altera Cyclone IV FPGA [28] is used to implement the supervising unit of the testing apparatus, whose principle schematic is shown in Fig. 7(b). A NIOS II embedded processor is used to interface the user PC with a time sequencer via an RS-232 standard bus. Such a sequencer is made up of several timers (white blocks in the figure), which have been concatenated in a proper way in order to produce the sequences in Fig. 7(a). For instance, at the end of t_{prot}, two time intervals begin, namely, T_{series} and T_{parallel}. The whole time sequence is initiated by the start signal generated by the processor. A connection matrix combines the signals coming from the timers to produce the four output signals. The above supervising unit adopts a 100-MHz oscillator, hence a 10-ns accuracy on times is achieved. Each timer is 32-b wide, so that a maximum time of ∼40 s can be set for each delay in Fig. 7(a).

III. Experiments

With the NDT described above, the behavior of a commercial IGBT power module under Type 1 short circuit was investigated, with special attention on the occurrence of oscillations on the gate and on its dependence on operating parameters. It is worth noting that all the tests have been performed at room temperature.

TABLE II
Main Specifications of the IGBT Module Under Test

Parameter	Value
Collector-emitter voltage, V_{CES}	1.7 kV
Continuous DC collector current, $I_{C,nom}$	1kA
Rated short circuit current, I_{SC}	4 kA
Gate-emitter peak voltage, V_{GES}	+/-20V
Internal gate resistance	1.5 Ω
Number of internal sections in parallel	6

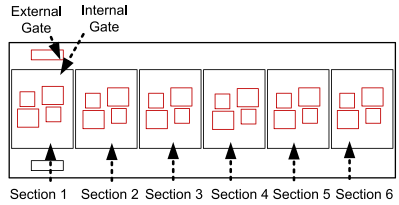


Fig. 8. Geometrical sketch of the studied 1.7-kV/1-kA IGBT power modules.

A. Device Under Test

The experiments are performed on several IGBT power modules from different manufacturers with the same rating (1.7 kV/1 kA) and same packaging style. The specifications have been reported in Table II. This module has six identical sections in parallel, as shown in Fig. 8. Each section includes two IGBT chips and two freewheeling diode chips in a half-bridge configuration. A customized ultramini CWT Rogowski probe has been adopted for current measurements due to its nonintrusive behavior (typical impedance in the range of a few picohenry) and its range of up to several kiloamperes [29].

B. Short-Circuit Tests at Different DC Voltage

Fig. 9 shows detailed waveforms of the same short-circuit test reported in Fig. 1. The test conditions were: 1) collector voltage 900 V; and 2) gate pulse duration 2.3 μs. The waveforms reported in Fig. 9 were obtained by increasing the gate pulse duration in steps until oscillations occurred. As is evident from both the figures, diverging oscillations can be found both on the gate voltage and on the collector voltage, taking place at ∼1.7 μs from the trigger instant, i.e., much earlier than the gate turn OFF edge. This observation suggests that such a phenomenon happens spontaneously, indicating an instability mechanism. It is worth noting that longer gate pulses would have led to the gate breakdown, as the oscillation amplitude kept diverging up to a dangerous value of ∼25 V (see Fig. 1). To check whether the oscillations are consistent with different samples, another three IGBT power modules with the same part number are tested, together with IGBT power modules of same rating from

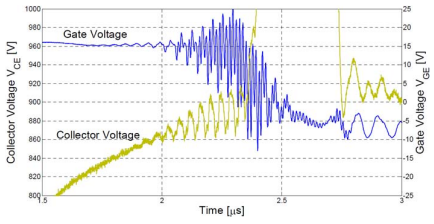


Fig. 9. Details of the short-circuit test performed in Fig. 1. Conditions: collector voltage $V_{CE} = 900$ V; gate pulse duration $t_{ON} = 2.3$ μs.

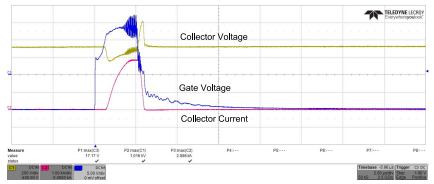
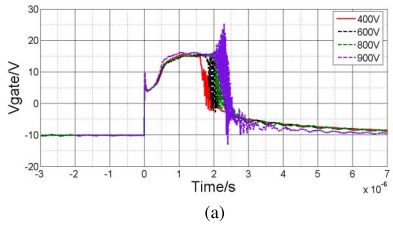


Fig. 10. Evidence of oscillations during a short-circuit test of a 1.7-kV/1-kA IGBT power module from another manufacturer performed at 700 V of collector voltage. Time scale: 2 μs/div. Gate voltage: 5 V/div. Collector voltage: 200 V/div. Collector current: 1 kA/div. The gate peak voltage was 17.17 V in this case.

different manufacturers. However, similar oscillations are detected for all the samples, and the testing result of another manufacturer's module is shown in Fig. 10.

To further investigate the dependence of the above phenomenon on the operating conditions, several more experiments have been performed at different collector voltages. Fig. 11(a) shows the gate waveforms obtained at increasing voltages from 400 to 900 V. Fig. 11(b) shows the detail of the same waveforms from $t = 0$ to $t = 2$ μs. The oscillation beginnings are indicated by arrows. Evidently, it appears from Fig. 11(b) that the oscillations commence after a time delay that increases with the applied voltage. Fig. 12 shows the relationship between this delay and the applied voltage for the complete set of the performed experiments. The delay clearly increases linearly with the applied voltage.

To better understand the observed oscillations, one open module has been tested at 800 V collector voltage. The internal gate voltage ($V_{\text{gate\_in}}$), which is measured on the IGBT chip, as well as the external gate voltage ($V_{\text{gate\_ex}}$), which is the gate driver output voltage (locations shown in Fig. 8), are shown in Fig. 13. Significantly different oscillation amplitudes can be observed in the time interval between $t = 2$ and $t = 3$ μs. It is worth noting that the oscillation amplitude at the internal gate is higher than the external one. A hypothesis is proposed that an amplification phenomenon takes place during oscillations, and the IGBT chip is the active part. Similar mechanism has also been suggested in [30], where oscillating phenomena have been evidenced during short circuit of discrete IGBTs.



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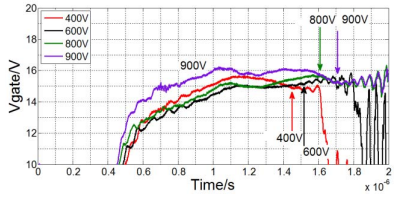


(b)

Fig. 11. Study of the oscillations' occurrence on the gate voltage at different collector–emitter voltages. (a) Gate voltage waveforms obtained at increasing collector voltages from 400 to 900 V. (b) Details of the same waveforms before the IGBT turn OFF from $t = 0$ to $t = 2$ μs.

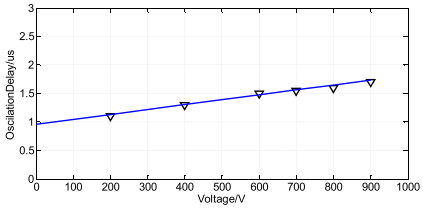


Fig. 12. Oscillation beginning delay versus collector voltage.

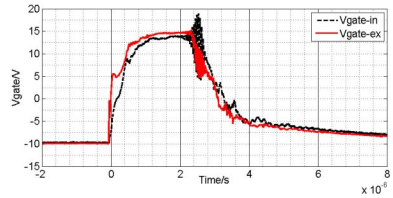
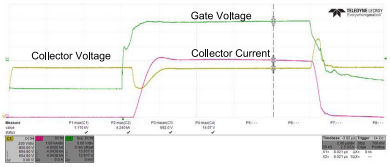


Fig. 13. Comparison between the external gate voltage ($V_{\text{gate-ex}}$) and the internal gate voltage ($V_{\text{gate-in}}$) in Fig. 11 during short circuit. Conditions: collector voltage 800 V.

C. Short-Circuit Tests With Different Circuit Stray Inductance

As widely suggested in the literature, the circuit stray inductance could play a major role in the triggering oscillation [21], [22]; therefore, the same tests have been repeated at a lower inductance value. To achieve this, the Schottky diodes have been removed from the circuit and the DUT lower side has been tested instead of the high side.



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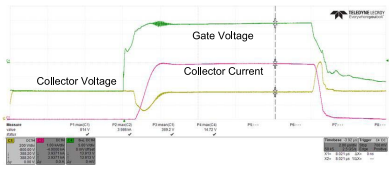


(b)

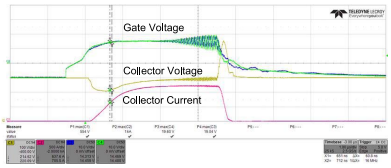
Fig. 14. Short-circuit tests performed at lower stray inductance $L_{\text{stray}} = 30$ nH. (a) Conditions: 700 V/10 μs. Time scale: 2 μs/div. Collector voltage (C1): 200 V/div. Collector current (C2): 1 kA/div. Gate voltage (C4): 5 V/div. (b) Conditions: 400 V/10 μs. Time scale: 2 μs/div. Collector voltage (C1): 200 V/div. Collector current (C2): 1 kA/div. Gate voltage (C4): 5 V/div.

Due to the terminal positions, the low side exhibits a little lower inductance than the high one. The estimated inductance in this case was $L_{\text{stray}} \approx 30$ nH. Fig. 14(a) shows a waveform obtained under this testing condition. Oscillations do not on the gate voltage or on the collector voltage anymore. The testing conditions are 700 V/10 μs. In the same experiment, the total collector current flowing through the module is with a peak value of 4.24 kA. Some oscillations, though, can be observed at a lower voltage, where they showed a dampened behavior. Fig. 14(b) shows a short-circuit test at 400 V showing some oscillations. Nevertheless, the peak value of the oscillating gate voltage in Fig. 14(b) is much lower than the value in Fig. 1.

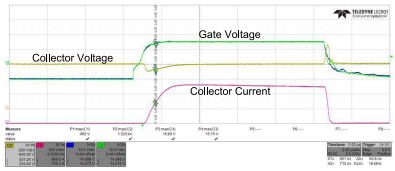
D. Short-Circuit Tests With Different Power Module Layout

The observed oscillations may also be related to internal stray parameters of the power module. Since there are six sections in parallel inside the studied 1700 V/1000 A power module, as plotted in Fig. 8, the parallel IGBT chips are connected by means of a dedicated busbar to the external terminals, which introduces stray elements network among the IGBT chips. This also implies there are interacting effects among IGBT chips during the high dynamic short-circuit situations.

To confirm the above hypothesis, additional tests with different internal layouts have been performed. First, a prototype with only two IGBT sections is fashioned from the same package by opening it and cutting away the connections to four of the six sections. Tests on it were conducted at several voltages and different short-circuit time durations. Oscillations could still be found at low-voltage conditions (300 V), but with much lower amplitudes than the full power module,



(a)



(b)

Fig. 15. Short-circuit waveforms for two parallel IGBT sections prototype module. (a) Conditions: 300 V/4 μs. Time scale: 1 μs/div. Internal gate voltage (C3): 10 V/div. External gate voltage (C4): 10 V/div. Collector voltage (C1): 100 V/div. Collector current flowing through two sections (C2): 500 A/div. (b) Conditions: 600 V/10 μs. Time scale: 2 μs/div. Collector voltage (C1): 200 V/div. Collector current flowing through two sections (C2): 500 A/div. Internal gate voltage (C3): 10 V/div. External gate voltage (C4): 10 V/div.

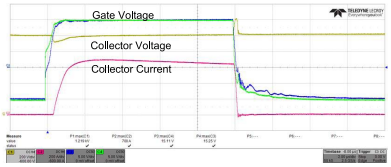


Fig. 16. Short-circuit waveforms for one IGBT section prototype module at 1000 V/10 μs. Time scale: 2 μs/div. Collector voltage (C1): 200 V/div. Collector current flowing through the section (C2): 200 A/div. Internal gate voltage (C3): 5 V/div. External gate voltage (C4): 5 V/div.

as shown in Fig. 15(a). The oscillations totally disappear at higher voltage (>400 V), and the test results at 600 V/10 μs are shown in Fig. 15(b). Following on from the above test, another prototype module with only one section was constructed and tested under short circuit. No oscillations could be observed throughout the whole voltage range (100–1000 V). The results at 1000 V/10 μs are shown in Fig. 16. The oscillations on the gate voltage are totally absent.

IV. Discussion on Mechanism of Triggering Oscillations

To better understand the mechanism provoking the oscillations, PSPICE simulations have been performed, including stray elements. The adopted IGBT model is a lumped charge IGBT model, which demonstrated good accuracy in short-circuit simulations [31]. Fig. 17 shows the circuit used where the stray inductance of the busbar connection L_{Cstray}, the stray inductance (L_{Estray}), and the

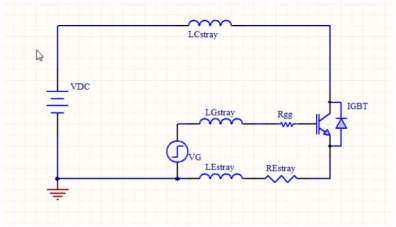


Fig. 17. PSPICE circuit adopted for simulations.

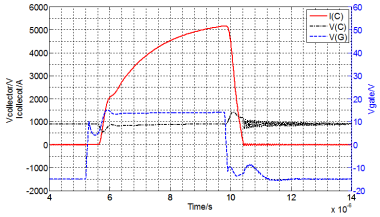


Fig. 18. Simulation output for the circuit in Fig. 17 in the same conditions in Fig. 1.

resistance (R_{Estray}) of the emitter lead and the stray components of the gate lead (L_{Gstray}, R_{gg}) are included. The parameters of the components have been measured from the real circuit except for the emitter leg ones, which have been estimated from the geometry of the physical module. Fig. 18 shows the simulation results under the same conditions as that of the experimental ones shown in Figs. 1 and 9. Even if the voltage and current were predicted in a good accuracy level, no oscillations took place. This suggests that a more powerful simulation tool is required.

On the other hand, a 2-D/3-D mixed-mode FEM simulation, including semiconductor physics, stray elements of the package, and the overall external circuit may not be feasible due to the large number of chips (six in this case) and the complex magnetic interactions at package level. For the above reason, an interpretation of the oscillations occurrence is given in an analytical way as follows.

Due to the large energy generated during a short circuit, the chip junction temperature cannot be assumed to remain constant. A large temperature peak in the order of 300 °C can typically occur [9]. Therefore, the above constant temperature PSPICE simulation cannot correctly predict what happens inside the device. Furthermore, the principal parameter involved in the signal amplification, i.e., the transconductance varies significantly with temperature but this effect is fully neglected if a constant temperature is assumed. The transconductance g is defined as

$$g = \frac{\partial I_C}{\partial V_{\mathrm{GE}}}|_{V_{\mathrm{GE}}=V_{\mathrm{GE0}}} \tag{1}$$

and it expresses the variation of the output collector current I_C in terms of the gate voltage V_{GE} at a specific gate bias V_{GE0}. This parameter strongly depends on the temperature and,

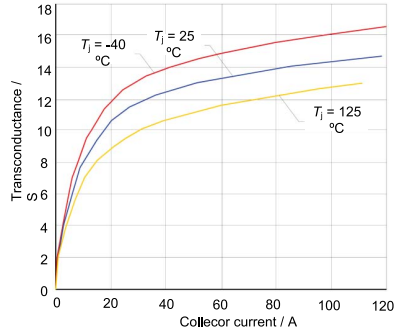


Fig. 19. Typical transconductance characteristics of a commercial IGBT at different junction temperatures [33].

specifically, decreases with increasing temperature [32] as

$$\frac{\partial g}{\partial T} < 0. \tag{2}$$

This result is a general one, as demonstrated by several manufacturers' application notes. For instance, in [33], the transconductance of the discrete IGBT devices is measured at different junction temperatures (−40 °C, 25 °C, and 125 °C) and the results have been reported in Fig. 19.

This temperature dependence aids the interpretation of the oscillations occurrence. Referring to Figs. 11 and 12, applied voltage influences the delay before oscillations commence. Assuming an exponential law in the amplitude of these oscillations, it can logically be observed that earlier oscillations behave like bigger ones. With the time constant τ, the oscillation amplitude at time $t + \Delta t$ can be obtained as

$$e^{\frac{t+\Delta t}{\tau}} = e^{\frac{t}{\tau}} \cdot e^{\frac{\Delta t}{\tau}} = K \cdot e^{\frac{t}{\tau}} \tag{3}$$

where

$$K = e^{\frac{\Delta t}{\tau}} > 1 \quad \text{if } \Delta t > 0. \tag{4}$$

Consequently

$$e^{\frac{t+\Delta t}{\tau}} > e^{\frac{t}{\tau}} \quad \text{if } \Delta t > 0. \tag{5}$$

A sketch of a typical short-circuit gate voltage waveform V_{GE} is reported in Fig. 20, in two different cases $V_{\mathrm{CE1}} < V_{\mathrm{CE2}}$, where $V_{\mathrm{CE1}} < V_{\mathrm{CE2}}$. Together with the corresponding oscillating gate voltage V_{GE1} and V_{GE2} waveforms, the junction temperature trend is also sketched in both cases, namely, T_1 and T_2. As $V_{\mathrm{CE1}} < V_{\mathrm{CE2}}$ and the current waveform is almost equal in both the cases, the power generated in the first case is lower than the second one, hence $T_1 < T_2$ along the entire transient duration. Moreover, from (2), the transconductance g decreases with temperature, so that $g_1 > g_2$. In the same figure, the trends of g_1 and g_2 are reported as well. The initial condition is supposed to be at room temperature, so that $g_1 = g_2 = g_{\mathrm{ROOM}}$ and $T_1 = T_2 = T_{\mathrm{ROOM}}$. Finally, there exists a given transconductance value g_{LIM}, below which oscillations disappear, i.e., a stability region.

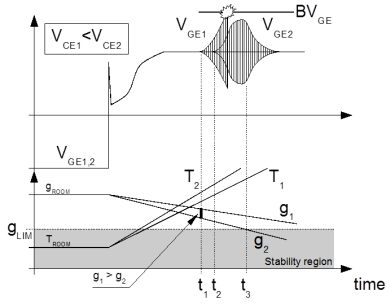


Fig. 20. Interpretation of the oscillation occurrence in terms of transconductance.

According to the experimental observation, oscillations at lower collector voltage take place earlier than the higher one, so V_{GE1} and diverges before V_{GE2}, and $T_1 < T_2$ in the picture. An interpretation of this experimental observation can be based on Fig. 20 and (5), because a lower temperature $T_1 < T_2$ leads to a higher transconductance $G_1 > G_2$, hence higher oscillation amplitudes, diverging oscillations take place earlier at lower collector voltage, i.e., at $T_1 < T_2$. It is worth noting that oscillations can eventually lead to the gate oxide breakdown if they reach the limit voltage BV_{GE}. Moreover, it could also be that the temperature rises so quickly that the transconductance goes into the stability region before the oscillations reach dangerous values (t_3 in Fig. 20). In this case, a spindle-shaped waveform appears on the gate voltage, similar to the one shown in Fig. 14(b).

This interpretation is in full agreement with the experimental observations at different voltages (i.e., Section III, B). Higher chip temperature happens at short circuits of higher collector voltages, which leads to consequent lower transconductance because of the temperature-dependence. Accordingly, the oscillations may occurrence later. As illustrated in experimental results in Fig. 12, the oscillation occurrence delay increases with collector voltage rising.

Finally, it is worth noting that stray parameters significantly affect the oscillations, and the diverging oscillations only happen at nonnegligible circuit stray inductance. The dependence of the oscillation occurrence on the stray inductance, both external and internal, can be finally explained by considering that the stability region boundary g_{LIM} depends on the circuit passive parameters, as is common in general electronic amplifiers.

V. Conclusion

A NDT rated at 6 kA/1.1 kV is used to investigate the short-circuit behavior of megawatt-scale IGBT power modules. Its main feature is to enable studying instabilities while protecting the DUT against explosions with a time resolution of 10 ns using FPGA hardware.

A comprehensive study has been performed on commercial IGBT power modules used in wind turbine applications to investigate the occurrence of unstable oscillations during short circuit. The results indicate a key role is played by the overall stray inductance: the diverging oscillations only happen at non-negligible circuit stray inductance. Furthermore, it is proposed that a decrease in the transconductance with temperature is the main mechanism causing the relationship between the time delays until oscillation occurrence and the applied voltage.

Acknowledgment

The authors would like to thank N. Baker for the valuable discussions.

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Rui Wu (S'13) received the B.Sc. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2009, and the M.Sc. degree in power electronics from the China Electric Power Research Institute, Beijing, China, in 2012. He is currently pursuing the Ph.D. degree with Aalborg University, Aalborg, Denmark.

He was with the China Electric Power Research Institute in 2012. His current research interests include multiphysics modeling of power devices and power device's behavior during abnormal conditions, in particular, short circuits.

Paula Diaz Reigosa (S'14) was born in Gijon, Spain. She received the B.S. degree in industrial engineering with a specialization in electrical engineering from the University of Oviedo, Oviedo, Spain, in 2012, and the M.S. degree in power electronics and drives from Aalborg University, Aalborg, Denmark, in 2014, where she is currently pursuing the Ph.D. degree in failure mechanisms for power semiconductor devices.

She joined Danfoss Power Electronics, Gråsten, Denmark, and Siemens Wind Power Systems, Brande, Denmark, for two different projects. Her current research interests include the reliability of power electronics, modeling, characterization of power semiconductor devices and simulation, wind turbines, and green power inverters.

Francesco Iannuzzo (M'01–SM'04) received the Ph.D. degree in electronics and information engineering from the University of Naples, Naples, Italy, in 2001, with a focus on the reliability of power MOSFETs during diode operations.

He is primarily specialized in power device modeling. He is a Full Professor of Reliable Power Electronics with Aalborg University, Aalborg, Denmark, where he is also part of the Center of Reliable Power Electronics. He has authored or co-authored over 90 publications in journals and international conferences. His current research interests include the reliability of power devices, including against cosmic rays, power device failure modeling, and development of nondestructive testing facilities for assessment of Megawatt-scale power modules under extreme conditions.

Prof. Iannuzzo is a Senior Member of the IEEE Reliability Society and the Industrial Electronic Society, and the Italian Electric, Electronic and Telecommunication Association.

Liudmila Smirnova (S'14) received the M.Sc. degree in electrical engineering from the Lappeenranta University of Technology (LUT), Lappeenranta, Finland, and Saint Petersburg Electrotechnical University, Saint Petersburg, Russia, in 2010. She is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, LUT.

Her current research interests include power electronics.

Huai Wang (S'07–M'12) received the B.Eng. degree in electrical and electronic engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2007, and the Ph.D. degree in electronics engineering from the City University of Hong Kong, Hong Kong, in 2012.

He was with the ABB Corporate Research Center, Baden, Switzerland, in 2009. He was a Visiting Scientist with ETH Zurich, Zurich, Switzerland, in 2014, and the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2013. He has been with Aalborg University, Aalborg, Denmark, since 2012, where he is currently an Assistant Professor with the Department of Energy Technology. He has contributed over 25 journal papers, and holds four patents. His current research interests include the reliability of dc-link and ac filter capacitors, reliability of power electronic systems, multiobjective life-cycle performance optimization of power electronic systems, high voltage dc–dc power converters, time-domain control of converters, and passive components reduction technologies, and their emerging power electronics applications.

Dr. Wang was a recipient of the six paper awards and project awards from the industry, the IEEE, and the Hong Kong Institution of Engineers. He was also a recipient of the Green Talents Award from the German Federal Ministry of Education and Research in 2014. He serves as a Guest Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issue on Robust Design and Reliability in Power Electronics, and the Session Chair of various conferences in power electronics.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) received the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 1992.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of Power Electronics and Drives in 1998. His current research interests include power electronics and its applications, such as wind turbines, Photovoltaics systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg has received 15 IEEE Prize Paper Awards. He was a recipient of the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award in 2014, and the Villum Kann Rasmussen Research Award in 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He was a Distinguished Lecturer of the IEEE Power Electronics Society from 2005 to 2007, and the IEEE Industry Applications Society from 2010 to 2011.

Publication 3

(*Journal Paper*)

Robustness of MW-Level IGBT Modules against Gate Oscillations under Short Circuit Events

Reigosa, Paula Diaz; Wu, Rui; Iannuzzo, Francesco; Blaabjerg, Frede

The paper has been published in the
Microelectronics Reliability, vol. 55, no. 9-10, pp. 1950-1955, Aug. 2015.

DOI:doi:10.1016/j.microrel.2015.07.011

Microelectronics Reliability 55 (2015) 1950–1955

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Robustness of MW-Level IGBT modules against gate oscillations under short circuit events

P.D. Reigosa [a,*], R. Wu [a], F. Iannuzzo [a,b], F. Blaabjerg [a]

[a] Center of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Pontoppidanstraede 101, 9220 Aalborg, Denmark
[b] DIEI, University of Cassino and Southern Lazio, Via G. Di Biasio 43, 03043 Cassino, Italy

ARTICLE INFO

Article history:
Received 26 May 2015
Received in revised form 30 June 2015
Accepted 3 July 2015
Available online 26 July 2015

Keywords:
Non-destructive testing
Short circuit
IGBT
Gate oscillations
Power electronics reliability

ABSTRACT

The susceptibility of MW-level IGBT power modules to critical gate voltage oscillations during short circuit events has been evidenced experimentally. This paper proposes a sensitivity analysis method to better understand the oscillating behavior dependence on different operating conditions (i.e., collector–emitter voltage, gate-emitter voltage and temperature). A study case on 1.7 kV/1 kA IGBT power modules is presented. The proposed study helps to understand the oscillation mechanism by revealing its relationship with different working conditions. Moreover, the study can be helpful to understand the oscillation phenomenon, as well as to further improve the device performance during short circuit.

1. Introduction

In high power applications, power semiconductor modules have been the most prevalent packaging. Insulated-Gate Bipolar Transistors (IGBTs) are the commonly used semiconductor devices, which can be configured in parallel to increase the current capability. One of the major challenges is to fulfill the product design specifications while continuously increase the lifetime expectation and the commutation speed. In modern power electronics systems, the ability of withstanding abnormal conditions (e.g. overloads and short circuits), is strictly required to achieve the lifetime specifications (e.g., at least 20 years for the MW-level wind turbine systems) [1,2].

Short circuit operations are very crucial for high power IGBT modules, as both high current and high voltage conditions are applied for several microseconds (i.e., typically less than 10 μs). Under specific operational conditions, high frequency gate-emitter voltage oscillations (i.e. tens of MHz) have been observed during both type 1 (turn-on transient) and type 2 (on-state) short circuits [3]. Such oscillations are very critical in case that the oscillation amplitude exceeds the maximum gate voltage provided on the manufacturer's datasheet — typically ±20 V. Exceeding this voltage may cause the breakdown of the gate oxide which will permanently damage the IGBT and therefore drastically limit the expected short circuit robustness.

Short circuit oscillations have been previously presented in the literature for single chip and parallel chip configurations, being more prone to occur in parallel chip configurations [4,5]. Different interpretations have been given depending on: a) the type of short circuit test (i.e., type 1 and type 2) [3], b) the starting point of the oscillations (i.e., on-state oscillations, turn-off oscillations) [6], c) the presence of negative capacitance under high temperatures and high collector voltages [7–10], d) the optimization of the layout design to suppress the oscillations [11–13], and e) the Plasma Extraction Transit Time (PETT) effect and the dynamic IMPact ionization Avalanche Transit-Time (IMPATT) effect as the excitation mechanisms for high frequency oscillations (i.e., hundreds of MHz) during the IGBT turn-off [14,15]. Even though the prior-art research discussed several oscillation mechanisms, another type of oscillation has been investigated in this paper for the first time.

Previous experimental observations conducted thanks to a 6 kA/1.1 kV Non-Destructive Tester (NDT) [16], led to conclude that there are three major aspects which significantly contribute to the oscillation phenomenon: a) a non-negligible DC-link inductance (i.e., several tens of nH), b) the internal layout design, that is, the stray parameters' network inside the module, and c) the IGBT chip characteristics (i.e., capacitance, switching speed and high frequency transconductance).

The aim of this paper is to investigate the oscillating behavior of MW-level IGBT power modules for type 1 short circuit, as well as reveal its relationship with the operating conditions (i.e., collector–emitter voltage, temperature and gate-emitter voltage). The study can be helpful

* Corresponding author.
E-mail address: pdr@et.aau.dk (P.D. Reigosa).

http://dx.doi.org/10.1016/j.microrel.2015.07.011
0026-2714/

to understand the oscillation phenomenon, as well as to further improve device's performances during short circuit.

2. Short circuit behavior on multi-chip IGBT power modules

2.1. Device Under Test

The experimental investigations were conducted on two commercial 1.7 kV/1 kA Trench-Gate Field-Stop IGBT power modules (Brand A and Brand B). Each module has 6 identical sections, whose electrical specifications based on the datasheet information are shown in Table 1. Each section contains two IGBT chips and two freewheeling diodes, which are configured as a half-bridge, as illustrated in Fig. 1a.

The internal stray parameters inside one section of the IGBT power module are illustrated in Fig. 1a. Due to the lack of information of the stray parameters, the Direct Bonded Copper (DBC) layout of one section of the IGBT power module has been extracted and its design layout has been used to build a Printed Circuit Board (PCB) as shown in Fig. 1b. The resistance and the inductance have been measured by means of an E4990A impedance analyzer. The results have been reported in Table 2.

2.2. Experimental results

The DUTs have been tested under a non-negligible DC-link inductance — 40 nH. The results show that a short circuit type 1 on the upper-arm IGBT power module exhibits high-frequency gate oscillations. Fig. 2 evidences the failure of the device in less than 2 μs and $V_{GE,peak} = 33\ V > 20\ V$.

In the experiments of Fig. 2, the gate and emitter terminals of the upper-arm IGBT were connected with a SCALE-2 driver (Concept 2SP0320V2A0) and the ones of the lower-arm IGBT were shorted. The internal gate voltage was directly measured on the IGBT chip and the external voltage was measured on the external lead. The internal gate oscillation amplitude is significantly higher than the external one implying that the IGBT chip contributes to the amplification phenomenon.

A deeper insight can be gained from Fig. 3a and Fig. 3b. The zoomed view helps to identify the non-sinusoidal oscillation characteristic during the short circuit test for both Brand A and B. The gate-emitter voltage is equal to +15/−10 V and the temperature of the module cases were at about 25 °C. The oscillations begin when the current reaches its saturation value with a frequency range about 20 MHz, and then, the oscillation amplitude diverges with time. Minor oscillations can be also observed on the collector voltage and the collector current.

3. Short circuit behavior on a single chip IGBT power module

3.1. Device Under Test

Short circuit tests have been performed on a single chip IGBT module in order to justify whether the oscillations are initiated by the chip itself. The 1700 V/150 A Trench-Gate Field-Stop IGBT module consists of a single half-bridge leg. The IGBT chip has similar characteristics as the ones in the 1.7 kV/1 kA modules. Table 3 shows its specifications.

Table 1
Device Under Test (DUT) specifications extracted from datasheets — 6 parallel sections.

Parameters	Brand A	Brand B
Collector–emitter voltage, V_{CES}	1.7 kV	1.7 kV
Collector current, $I_{C,nom}$	1 kA	1 kA
Turn-on energy loss, E_{on}	390 mJ	400 mJ
Turn-off energy loss, E_{off}	295 mJ	270 mJ
Collector saturation voltage, $V_{CE(sat)}$	2.40 V	2.35 V
Gate threshold voltage, $V_{GE(th)}$	5.8 V	5.8 V

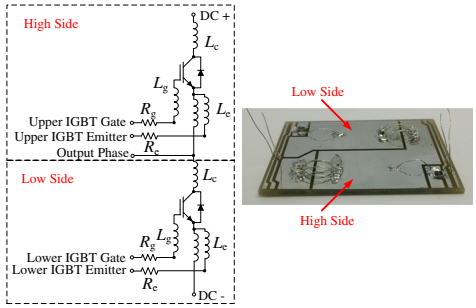

Fig. 1. Single section internal stray parameters of the IGBT power module: (a) circuit, and (b) Printed Circuit Board.

3.2. Experimental results

The following investigations have been done with the help of single-chip measurements. A commercial 1700 V/150 A half-bridge IGBT has been tested. Similarly, the gate and emitter terminals were connected with a SCALE-2 driver (CONCEPT). The turn-on and turn-off gate resistances were increased accordingly, however the DC-link inductance remained unchanged (40 nH).

The results in Fig. 4 show again the evidence of oscillations with unstable amplitude (i.e., diverging and converging repeatedly). The results confirm that it is not a chip-to-chip oscillation, so that the oscillations are coming from the chip itself. The oscillation frequency is about 20 MHz at low DC-link voltages. On the other hand, the oscillations are not observed at higher DC-link voltages (i.e., from 400 V up to 800 V).

4. Sensitivity analysis of gate oscillations during short circuit

Besides the key factors triggering the observed oscillations (i.e., DC-link inductance, IGBT chip characteristics and internal layout design), there is also a dependency on the testing conditions. Thus, the goal is to carry out a sensitivity analysis on the oscillating behavior's dependence on different working conditions, such as, gate-emitter voltage, temperature and collector-emitter voltage. The analysis is carried on the 1.7 kV/1 kA power module.

4.1. Oscillation dependence on gate-emitter voltage

In practical applications, the manufacturer recommends a positive gate voltage of 15 V to ensure high switching efficiency, 10 μs short circuit withstanding capability and long-term reliability. In general, the short circuit current is specified in the manufacturer's datasheet for a specific DC-link voltage, gate voltage of 15 V and specific junction temperature. However, in real applications the short circuit current may be higher than the value stated in the datasheet due to different operating conditions. The experimental observations presented above

Table 2
The estimated stray inductance and resistance.

Parameters	High Side	Low Side
Gate inductance, L_g	17 nH	19 nH
Emitter inductance, L_e	34 nH	37 nH
Gate resistance, R_g	21 mΩ	22 mΩ
Emitter resistance, R_e	19 mΩ	28 mΩ
Collector inductance, L_c	11 nH	11 nH

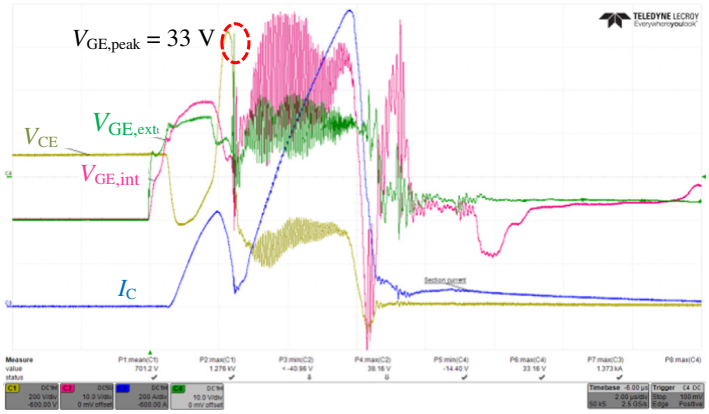

Fig. 2. Failure due to high gate voltage oscillations of 1.7 kV/1 kA IGBT short circuit: V_{CE} = 200 V/div, V_{GE} = 10 V/div, I_C = 200 A/div and t = 2 μs/div.

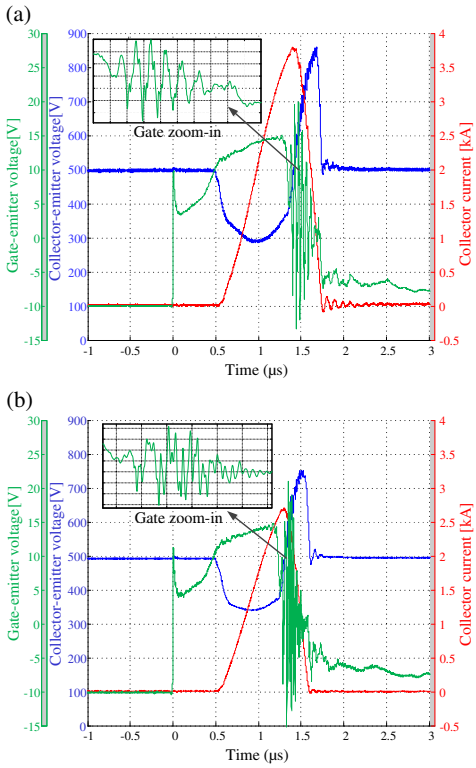

Fig. 3. Short circuit test of the 1.7 kV/1 kA IGBT power module (500 V/1.3 μs): (a) Brand A, and (b) Brand B.

pointed out that the maximum allowable gate voltage ($V_{GES} = \pm 20$ V) is exceeded when the device is operated at $V_{GE} = 15$ V. In order to overcome this problem, a reduced transconductance of the IGBT can be achieved by reducing the driving gate voltage (e.g., $V_{GE} = 14$ V), so that a smaller amplification is expected. Several short circuit tests were conducted on the upper-arm of a 1.7 kV/1 kA IGBT power module at different DC-link voltages, whose case temperature (T_{case}) was kept at about 25 °C, whereas the gate voltage was set at 14 V and 13 V. For the sake of brevity, only one short circuit test is shown in Fig. 5. In order to characterize the oscillation dependence on the gate-emitter voltage, two figures-of-merits are evaluated. The first one named the *oscillation factor* (Φ), measures the energy of the observed oscillation, that is, the square root of the AC signal within the oscillation interval (i.e., from 1 μs up to 10 μs):

$$\Phi = \sqrt{\frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \left[X(t) - V_{GE,ext}\right]^2} \tag{1}$$

where, Φ is the oscillation factor, $V_{GE,ext}$ is the applied gate voltage and t_1–t_2 is the time interval. It can be clearly seen from Fig. 6a that the oscillation factor is smaller for lower gate voltages. The second figure-of-merit characterizes the gate voltage peak $V_{GE,peak}$ at different DC-link voltages. Fig. 6b shows a randomness dependency, but significantly smaller than the previous experiments at $V_{GE} = 15$ V.

4.2. Oscillation dependence on temperature

The change in temperature influences the inherent characteristics of semiconductor devices, therefore higher temperature results in lower speed commutations, higher switching energy losses, lower threshold

Table 3
Device Under Test (DUT) specifications extracted from the datasheet — half-bridge IGBT.

Parameters	Value
Collector–emitter voltage, V_{CES}	1.7 kV
Collector current, $I_{C,nom}$	150 A
Turn-on energy loss, E_{on}	50 mJ
Turn-off energy loss, E_{off}	47 mJ
Collector saturation voltage, $V_{CE(sat)}$	2.40 V
Gate threshold voltage, $V_{GE(th)}$	5.8 V

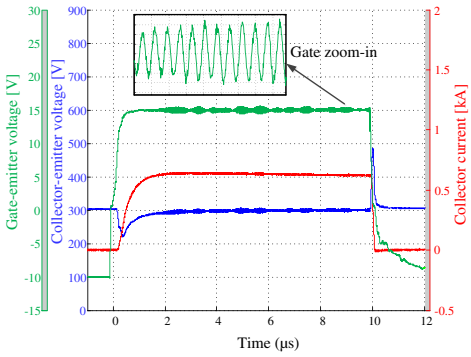

Fig. 4. Short circuit test of the 1700 V/150 A half-bridge IGBT (300 V/10 μs).

voltages and lower transconductance. The 1.7 kV/1 kA IGBT module has been tested under the case temperatures of 50 °C and 80 °C. Fig. 7 illustrates a short circuit at 800 V/10 μs and T_{case} = 80 °C.

In this case, the oscillation shape is different from Fig. 5; oscillations diverge and converge repeatedly. The most appropriate figure-of-merit is the gate voltage peak (Fig. 8), which clearly shows that lower gate voltage peaks can be achieved at higher temperatures. On the other hand, the *oscillation factor* is not a good measure because the oscillation does not definitively converge as in the previous cases.

5. Analysis of variations in the oscillation frequency

A significant result comes out from the observation of the oscillation frequency. The measured frequency is investigated for the two case studies (gate-emitter voltage and temperature). The increasing tendency of the oscillation frequency is observed for both cases, as shown in Fig. 9a and b.

The oscillation frequency increases with the applied DC-link voltage, whose interpretation arises from the influence of the transfer Miller capacitance [12]. The Miller capacitance, C_{GC}, has a non-linear characteristic with the applied collector–emitter voltage, so that its value decreases if the collector–emitter voltage is increased; hence a higher oscillation frequency is expected.

In addition, an interesting observation can be made with reference to Fig. 9b. As the temperature increases, the oscillation frequency decreases. The half-bridge circuit depicted in Fig. 10 contains two possible resonant circuits: (a) the gate drive loop, and (b) the power loop. The following analysis justifies that the oscillation frequency dependence

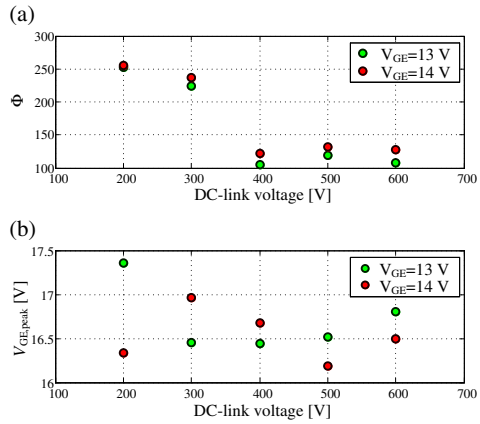

Fig. 6. (a) Oscillation factor and (b) gate voltage peak comparison at 25 °C.

with temperature seems not to be correlated with the parasitic parameters in both loops.

Based on Kirchhoff's laws and neglecting the current coming from the power loop, the gate drive loop can be expressed by using the following equations extracted from Fig. 10:

$$i_1 - i_2 - i_3 = 0 \tag{2}$$

$$V_{IN} = i_1 R_g + L_g \frac{di_1}{dt} + \frac{1}{C_{GE}} \int i_3 \, dt \tag{3}$$

$$V_{CE} = \frac{1}{C_{CE}} \int i_2 \, dt \tag{4}$$

$$V_{CE} = -\frac{1}{C_{GC}} \int i_2 \, dt + \frac{1}{C_{GE}} \int i_3 \, dt \ . \tag{5}$$

The transfer function of the input gate signal and the output collector–emitter voltage can be expressed as:

$$\frac{V_{CE}(s)}{V_{IN}(s)} = \frac{1/A}{s^2 + (2sC_{GE}R_gC_{CE})/A + (C_{CE} + C_{GC})/A} \tag{6}$$

where; $A = L_g(C_{GE}C_{GC} + C_{GE}C_{CE} + C_{GC}C_{CE})$.

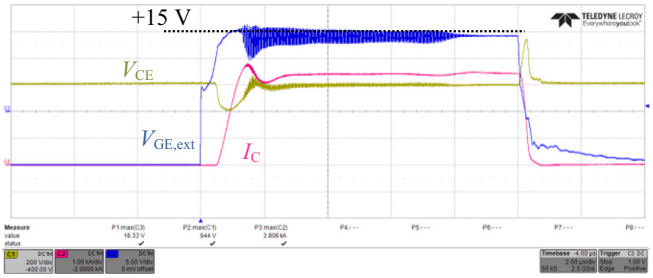

Fig. 5. Gate oscillations during 600 V/10 μs short circuit of the 1.7 kV/1 kA IGBT: V_{GE} = 14 V & T_{case} = 25 °C (V_{CE} = 200 V/div, V_{GE} = 5 V/div, I_C = 1 kA/div and t = 2 μs/div).

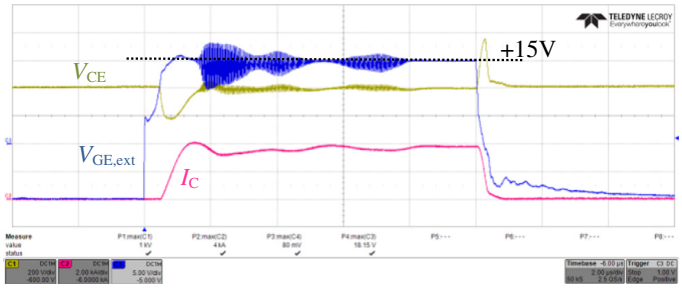

Fig. 7. Gate oscillations during 800 V/10 μs short circuit of the 1.7 kV/1 kA IGBT: $V_{GE} = 15$ V & $T_{case} = 80$ °C ($V_{CE} = 200$ V/div, $V_{GE} = 5$ V/div, $I_C = 2$ kA/div and $t = 2$ μs/div).

Therefore, the oscillation frequency, ω_n, can be expressed as:

$$\omega_n = \sqrt{\frac{C_{CE} + C_{GC}}{L_g(C_{GE}C_{GC} + C_{GE}C_{CE} + C_{GC}C_{CE})}}. \quad (7)$$

On the other hand, the total loop inductance, L_{module}, (the sum of L_e, L_c and $L_{DC\text{-}link}$) and the output capacitance, C_{oss}, (the sum of C_{GC} and C_{CE}) form a resonant circuit and causes oscillations in a short period after turn-on. The oscillation frequency could be determined as:

$$f = \frac{1}{2\pi\sqrt{L_{module}C_{oss}}}. \quad (8)$$

As it can be observed from Eqs. (7) and (8), the higher the inductance; the lower the expected frequency. According to the literature, higher temperatures result in lower inductance [17], whereas the Miller and junction capacitances are stable with temperature [18]. This means that if the temperature increases, higher frequencies are expected, which is not in agreement with the measurements. This contradictory result reinforces that the oscillations are due to inherent mechanisms of the chip itself.

6. Discussion

The short circuit robustness of MW-level IGBT power modules may be compromised with the development of new technologies aiming for fast switching semiconductors and higher current capability. The observed gate voltage oscillations have a non-sinusoidal characteristic, differing from the ones produced by an LC-circuit. This leads to the assumption that the oscillation may be initiated and sustained by the IGBT chip.

Since the transconductance of the IGBT may be involved, PSpice short circuit simulations are performed at a specific gate bias V_{GE0} with an accurate physics-based IGBT model based on the Lumped-Charge method. Then, a small amplitude sinusoidal signal (e.g. tens of mV-level) at a given frequency is supplied to the V_{GE}, the corresponding variation of the output collector current I_C can be obtained. The transconductance at the given frequency can be calculated by means of Eq. (9):

$$g = \frac{\partial I_C}{\partial V_{GE}}\bigg|_{V_{GE}=V_{GE0}}. \quad (9)$$

In Fig. 11 can be seen that the transconductance decreases with temperature rising at the frequency below MHz-level. However, it also illustrates a reduced transconductance in the range above 10 MHz, which is not temperature dependent anymore. It means that the IGBT is not able to amplify the input signal anymore and thus another mechanism is causing the oscillations to diverge. Recently, it has been discussed that IGBT chips are unstable due to the evidence of negative gate capacitance values. This hypothesis is excluded because the oscillations are less critical at high collector–emitter voltages and an increase of temperature helps to damp the oscillation, opposite to the negative capacitance phenomenon.

Moreover, the observed oscillation frequency is about 20 MHz, it seems not to be correlated with other electromagnetic disturbances such as Transit Time oscillations (e.g., 200 MHz).

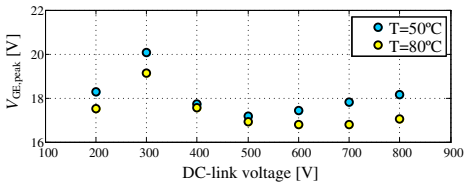

Fig. 8. Gate voltage peak comparison with different T_{case} at $V_{GE} = 15$ V.

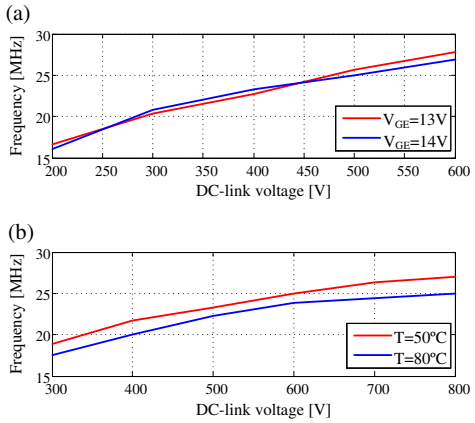

Fig. 9. Oscillation frequency comparisons: (a) $T_{case} = 25$ °C, and (b) $V_{GE} = 15$ V.

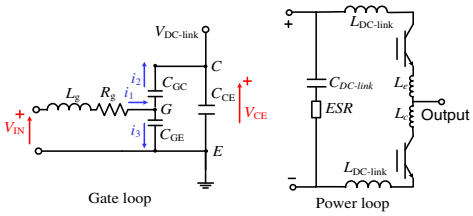

Fig. 10. Equivalent circuit of a half-bridge circuit.

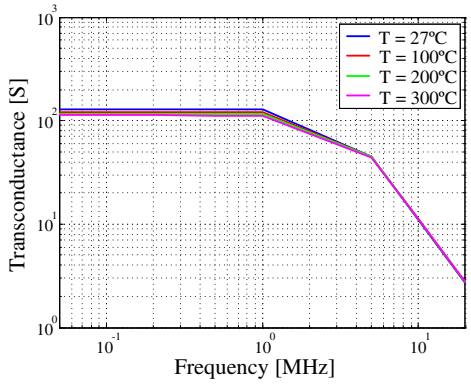

Fig. 11. Simulated transconductance with frequency at different temperature conditions.

7. Conclusions

The analysis in this paper has revealed a new oscillation phenomenon which takes place on the MW-level IGBT modules under type 1 short circuit. The observed oscillations appear for single-chip and parallel-chip configurations, being more critical in parallel-chip configurations due to possible positive feedbacks involving the stray parameters of the module. Thanks to the sensitivity analysis on the oscillating behavior's dependence on different working conditions, the factors which help to minimize the oscillations can be pointed out: low gate-emitter voltage, high temperature and high collector–emitter voltage.

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Conference Papers

Publication 4

(*Conference Contribution*)

Catastrophic Failure and Fault-Tolerant Design of IGBT Power Electronic Converters - An Overview

Wu, Rui; Blaabjerg, Frede; Wang, Huai; Liserre, Marco; Iannuzzo, Francesco

The paper has been published in the
Proceedings of the 39^{th} *Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, pp. 507-513, 2013.

DOI:10.1109/IECON.2013.6699187

Catastrophic Failure and Fault-Tolerant Design of IGBT Power Electronic Converters - An Overview

Rui Wu, Frede Blaabjerg, Huai Wang, Marco Liserre
Center of Reliable Power Electronics (CORPE)
Department of Energy Technology, Aalborg University
Pontoppidanstraede 101, 9220 Aalborg, Denmark
rwu@et.aau.dk, fbl@et.aau.dk, hwa@et.aau.dk,
mli@et.aau.dk

Francesco Iannuzzo
Department of Electric and Information Engineering
University of Cassino and southern Lazio
Via G. Di Biasio, 43 03043 Cassino, Italy
iannuzzo@unicas.it

***Abstract*—Reliability is one of the key issues for the application of Insulated Gate Bipolar Transistors (IGBTs) in power electronic converters. Many efforts have been devoted to the reduction of IGBT wear out failure induced by accumulated degradation and catastrophic failure triggered by single-event overstress. The wear out failure under field operation could be mitigated by scheduled maintenances based on lifetime prediction and condition monitoring. However, the catastrophic failure is difficult to be predicted and thus may lead to serious consequence of power electronic converters. To obtain a better understanding of catastrophic failure of IGBTs, the state-of-the-art research on their failure behaviors and failure mechanisms is presented in this paper. Moreover, various fault-tolerant design methods, to prevent converter level malfunctions in the event of IGBT failure, are also reviewed.**

Keywords—Insulated Gate Bipolar Transistor; catastrophic failure; fault torlerant circuit; power electronics

I. INTRODUCTION

Nowadays, power electronics play an important role in motor drives, utility interfaces with renewable energy sources, power transmission (e.g. high-voltage direct current systems, and flexible alternating current transmission systems), electric or hybrid electric vehicles and many other applications. Therefore, the reliability of power electronics becomes more and more vital, and should draw more attention [1]. According to a survey, semiconductor failure and soldering joints failure in power devices take up 34% of power electronic system failures [2]. Another survey shows that around 38% of the faults in variable-speed ac drives are due to failure of power devices [3]. A recent questionnaire on industrial power electronic systems also showed that all the responders regard power electronic reliability as an important issue, and 31% of the responders selected the "semiconductor power device" as the most fragile component [4]. It can be seen that studying the reliability of power devices is important.

Insulated Gate Bipolar Transistors (IGBTs) are hybrid bipolar-metal-oxide semiconductor, which have the advantages of low on-state resistance, voltage control of the gate and wide safe operating area. IGBTs are also one of the most critical components as well as the widely used power devices in power electronic systems in the range above 1 kV and 1 kW. According to the survey, the most used power devices for industrial applications are IGBTs [4]. Therefore it is worth investigating IGBT's failure and exploring the solutions to improve the reliability of IGBT power electronic converters.

The failure of IGBTs can be generally classified as catastrophic failure and wear out failure. IGBT wear out failure is mainly induced by accumulated degradation with time, while catastrophic failure is triggered by single-event overstress, such as overvoltage, overcurrent, overheat and so on. Prognostics and Health Management (PHM) method can monitor the degradation of IGBTs and estimate wear out failure [5]. However, PHM is not applicable for catastrophic failure, which is more difficult to be predicted.

Several overview papers have covered the topics on IGBT failure and fault diagnosis, and protection methods [6-12].

In [6], C. Busca *et al* discuss the major wear out failure mechanisms of IGBTs in wind power application. It covers the bond wire lift-off, solder joint fatigue and bond wire heel cracking due to coefficients of thermal expansion (CTEs) mismatch, aluminum reconstruction, and cosmic ray induced failure for IGBT modules. The fretting damage, spring fatigue, spring stress relaxation and cosmic ray induced failure of press-pack IGBTs are summarized. The aforementioned failure mainly occurs due to long time operation or power/thermal cycling, which can be classified as wear out failure, while no catastrophic failure is investigated.

In [7], M. Ciappa gives a comprehensive overview on IGBT module wear out failure mechanisms, such as bond wire fatigue, aluminum reconstruction, substrate cracking, interconnections corrosion, and solder fatigue and voids, while IGBT catastrophic failure is not discussed in detail except for the mechanism of latch-up. In particular, the bond wire lift-off mechanism is also discussed and modeled in [8].

In [9], S. Yang *et al* review the condition monitoring for semiconductor devices in power electronic converters. Some general failure mechanisms of power devices are also described. Bond wire lift-off and solder fatigue are investigated in detail, while only latch-up, gate oxide breakdown are mentioned for IGBT catastrophic failure. Diagnosis and prognosis methods for power devices degradation are also investigated.

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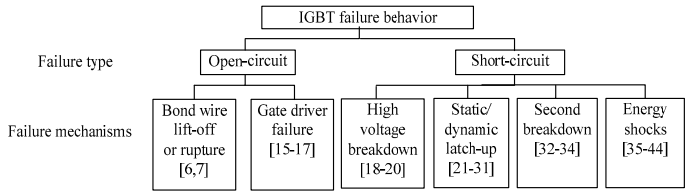

Fig. 1. Overview of IGBT catastrophic failure.

In [10], J. Flicker *et al* discuss IGBT failure in detail, including all wear out failure mechanisms mentioned above, as well as some catastrophic short-circuit failure mechanisms. However, the failure mechanisms such as second breakdown, high voltage breakdown and the open-circuit catastrophic failure have not been covered.

IGBT failure is also generally mentioned in references [11] and [12], which are more focused on IGBT fault diagnosis, detection and protection methods.

As discussed above, previous review papers on IGBT failure are mainly focused on wear out failure. A detailed and comprehensive review on IGBT catastrophic failure is still lacking, though. Moreover, it is also worth having an overview on the fault-tolerant designs to deal with or isolate IGBT catastrophic failure in power electronic converters.

Therefore, the aim of this paper is to provide an unbiased review of the major types of IGBT catastrophic failure due to overstresses and the corresponding fault-tolerant designs to deal with the failure at converter level. The paper is organized as follows: Section II classifies the IGBT catastrophic failure types. Section III summarizes the catastrophic failure of IGBTs in terms of failure mode and failure mechanism. Section IV discusses modern redundancy techniques for catastrophic failure tolerance. The detailed mechanisms of the fault tolerant circuits are also illustrated. The concluding remarks are summarized in Section V.

II. Classification of IGBT Catastrophic Failure

IGBT catastrophic failure behaviors can be classified as open-circuit failure and short-circuit failure. Normally, open-circuit failure is considered as not fatal to converters, since the converter can operate with lower quality of output. On the contrary, short-circuit failure is almost fatal to converters, as the uncontrolled short-circuit current may destroy the failed IGBT and/or other components in the circuit. IGBT catastrophic failure can be classified as shown in Fig. 1.

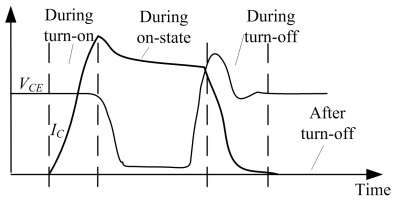

Fig.2. Time-sequence classification of IGBT short-circuit failure.

A. Open-circuit Failure

IGBT open-circuit failure can happen after external disconnection due to vibration, as well as bond wires lift-off or rupture due to high short-circuit current. It may lead to pulsating current, output current/voltage distortion, and result in secondary failure of other components after some time. Open-circuit can also be due to absence of gate drive signal. The common reasons could be the damage of components in drivers and the disconnection between driver board and IGBTs.

B. Short-circuit Failure

IGBT short-circuit failure modes can be classified with respect to time-sequence as shown in Fig. 2 [13]. IGBT short circuit during turn-on can be caused by high gate voltage and external failure. Failure during on-state may be caused by static latch-up or the rapid increase of intrinsic temperature caused by second breakdown, as well as by energy shocks. Failure during turn-off can be caused by dynamic latch-up and high voltage breakdown. Failure during off-state may be due to thermal runaway phenomenon. The detailed failure mechanisms will be illustrated in the next section.

III. IGBT Catastrophic Failure Mechanisms

Generally, catastrophic failure mechanisms are more related to semiconductor physics and overstress working conditions. As mentioned in Fig. 1, there are two failure mechanisms of open-circuit and four of short-circuit failure.

A. Open-circuit Failure Mechanisms

IGBT open-circuit failure is not fatal to the converter immediately, but may result in secondary failure in other devices and the converter. The mechanisms are as follows:

1) Bond wire lift-off or rupture.

Bond wire lift-off failure can happen after short-circuit failure. It is generally due to mechanical reasons. The main mechanisms are related to mismatch of coefficients of thermal expansion (CTEs) between Silicon and Aluminum, together with high temperature gradients. Crack initiates at the periphery of the bonding interface, and the bond wire finally lifts-off when crack propagates to the weaker central bond area [14]. Central emitter bond wires normally fail first, and then the survivor bond wires follow. Another failure mechanism is bond wire rupture, which is slower than lift-off and usually observed after long power cycling tests [7].

2) Gate driver failure.

There are various causes of gate driver failure, such as power stage devices (e.g. BJTs or MOSFETs) damaged; wires between drive board and IGBT disconnected [15]. The driver failure may result in IGBT intermittent misfiring, degraded output voltage, and overstress of other IGBTs and capacitors.

Abnormal work conditions in power terminals of IGBT can also lead to driver failure. Continued narrow overvoltage spikes between collector and emitter may open the gate-emitter resistance, while over-current of IGBT's collector may lead to gate-emitter resistance degradation [16]. Gate open-circuit failure can result in thermal runaway or high power dissipation [17]; however detailed research on the physical failure mechanism is still lacking. Moreover, modern IGBTs can work at 175°C junction temperature, which means the case temperature could reach 100°C or more, while most components in the driver cannot work normally at such high temperature. Thus this is a challenge for gate driver working at high temperature.

B. *Short-circuit Failure Mechanisms*

IGBT short-circuit failure can lead to potential destruction to the failed IGBT, remaining IGBTs, and other components, as it induces uncontrolled high current through the circuit. As shown in Fig.1, short-circuit failure can be classified as the following four different types.

1) High voltage breakdown.

High voltage spikes induced by high falling rate of collector current (I_C) and stray inductance can destroy IGBT during turn-off, especially under repetitive spikes [18,19]. Due to the high turn-off voltage spike, electric field can reach the critical field and break down one or a few IGBT cells first, and lead to high leakage current as well as high local temperature. Subsequently, the heat-flux radially diffuses from the over-heated region to the neighboring cells. Collector-emitter voltage (V_{CE}) collapses after the voltage spike, and then I_C rises again. Also, the gate terminal may also fail, which results in gate voltage (V_{GE}) rising up.

High value of V_{CE} and V_{GE} can also lead to short-circuit during turn-on. An abrupt destruction and peak current happen after several microseconds during turn-on. The hole current caused by avalanche generation concentrates on a certain point (usually high-doped p+ region). The destruction point is always located at the edge of the active area close to device's peripheral region [20]. Therefore, it is critical to clamp V_{GE} and V_{CE} during switching transients.

2) Static/ dynamic latch-up.

Latch-up is a condition where the collector current can no longer be controlled by the gate voltage. With respect to Fig. 3, latch-up happens when the parasitic NPN transistor is turned on, and works together with the main PNP transistor as thyristor, and then the gate loses control of I_C. IGBT latch-up can be divided into two types, static and dynamic latch-up [21].

Static latch-up happens at high collector currents, which turn on the parasitic NPN transistor by increasing the voltage drop across the parasitic resistance R_S.

Dynamic latch-up happens during switching transients, usually during turn-off, when the parasitic NPN transistor biased by the displacement current through junction capacitance C_{cb} between the deep P+ region and the N-base region. There are two distinct conditions that may lead to dynamic latch-up [22-27]. One is when the gate voltage drops very fast and induces excessive displacement current through the gate oxide that flows through the parasitic resistance. The other one is when the off-state collector-emitter voltage is quite high and induces excessive charging currents within the IGBT during the switching transient, which will flow through the parasitic resistance. Both conditions may trigger the parasitic NPN transistor and eventually lead to latch-up. It should be noticed that the collector current leading to dynamic latch-up is lower than that of static latch-up.

When latch-up happens, IGBT will be almost inevitably damaged due to the loss of gate control, as confirmed by the 2D finite element simulations [28,30]. Therefore, several methods are proposed to predict latch-up, especially based on the collector-emitter on-voltage $V_{CE(on)}$ and turn off time [28,29].

It is worth mentioning, though, that latest-generation IGBTs with trench-gate structure and heavily doped P-base region under N-emitter, have been proved to have good latch-up immunity [31], and latch-up is not a common failure in the latest devices anymore.

3) Second breakdown.

Second breakdown is a kind of local thermal breakdown for transistors [32] due to high current stresses, which can also happen to IGBTs during on-state and turn-off.

The failure mechanism of second breakdown is as follows: with the increase of current, the collector-base junction space-charge density increases, and the breakdown voltage decreases, resulting in a further increase in the current density. This process continues until the area of the high current density region reduces down to the minimum area of a stable current filament. Then, the filament temperature increases rapidly due to self-heating and a rapid collapse in voltage across IGBT occurs. This has been comprehensively simulated and measured in [33]. How to improve IGBT ruggedness at high current density and prevent second breakdown is still an interesting research topic [34].

4) Energy shocks.

During short circuit at the on-state, failure may happen due to high power dissipation. The high power dissipation within a short time is defined as energy shock. The high short-circuit

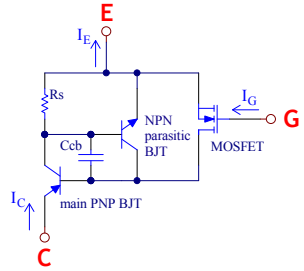

Fig. 3. The equivalent circuit of IGBT [21].

TABLE I. SUMMARY OF IGBT SHORT-CIRCUIT FAILURE MECHANISMS

Failure Mechanisms	Failure Behavior	Failure Location	Thermal Behavior
High voltage breakdown	During turn-off: V_{CE} collapses and I_C rises after voltage spike	At the edge of active area	Overheating on few peripheral cells at first, and then spreads to the whole chip
	During turn-on: peak I_C results in destruction		
Latch-up	Static latch-up during on-state: high I_C leading to loss of gate control	Active area	Overheating on a stable subset of cells of the device
	Dynamic latch-up during transients: high dv/dt leading to loss of gate control		
Second breakdown	Local thermal breakdown due to high currents	Emitter regions	Very high local temperature spots
Energy shocks	$E>E_C$: thermal runaway after successfully turned-off	Emitter regions	Very high local temperature spots
	$E<E_C$: degradation of die metallization	Al metallization layer, bond wires lift-off	Local overheating of Al metallization layer after 10^4 cycles

current will result in energy shock and high temperature [35,36]. However, IGBT will not immediately fail even the junction temperature exceed the rated temperature. Until reaching the intrinsic temperature (about 250°C for the doped silicon), further rise in junction temperature would lead to exponential increase in the carrier concentration and thermal runaway. With further increase of temperature, the silicon die may become fatally damaged and the contact metal may also migrate into the junctions.

Even the short-circuit current is successfully turned-off, short-circuit failure could still happen after several microseconds, which is called delayed failure in [31]. It is verified by experiments and numerical simulation that large leakage current leads to the thermal runaway [37]. A "critical energy (E_C)" is proposed to explain the mechanisms of catastrophic failure and wear out failure under repetitive short-circuit operations [38]. When short-circuit energy is below E_C, IGBT may survive for more than 10^4 times repetitive short-circuit operations before failed. However, when short-circuit energy is far beyond E_C, IGBT may fail after first short-circuit due to thermal runaway. A further experimental investigation show that IGBT can turn-off successfully after short-circuit but fails after several microseconds when the short-circuit energy is lightly higher than E_C. It is still challenging to determine the exact value of E_C, even though many experiments and numerical simulations have been done in the prior-art research [38,39].

A recent research also demonstrates this failure mechanism in trench gate field-stop structure IGBT by comprehensive experiments [40]. Since trench-gate field-stop IGBT has a smaller heat capacity [31,37], a state-of-the-art process has been proposed which can increase E_C by 80% according to simulations [41]. The basic principle is to use a thicker front side metallization, made of copper instead of aluminum, and a newly developed diffusion soldering process to attach the direct bonded copper (DBC) substrates.

Furthermore, it is worth mentioning that IGBTs can fall into short-circuits due to external causes, like the dynamic avalanche of freewheeling diodes; therefore it is also crucial to design high performance freewheeling diodes [42-44].

A summary of IGBT short-circuit failure mechanisms is presented in Table I. As discussed before, short-circuit currents inevitably introduce high energy and temperature to IGBT chips, therefore it is important to design an efficient thermal management to improve the ability of withstanding short-circuits in order to have time to detect failure and protect IGBTs.

IV. FAULT-TOLERANT CIRCUITS

Broadly speaking, it is worth to note first as a general principle that whatever fault-tolerant circuit or topology adds complexity and cost to the converter, and may fail by itself. For this reason, the final reliability-level is a trade-off between enhancing fault tolerance and increasing weaknesses. With the above in mind, different fault-tolerant designs at circuit level have been proposed, which are classified as shown in Fig. 4.

A. Device Redundancy

Contrary to modules, press-pack IGBTs intrinsically short after a catastrophic failure, due to the absence of bond wires and direct connection between die and metal contacts [45]. This feature can be profitably used for series redundancy, where several devices work as a single-switch. Nowadays it is widely used in traction, high power drives and power transmission systems [46,47]. However, for the sake of completeness, it should be pointed out that failed press-pack IGBTs could be open-circuit after some time, due to the interaction of molten aluminum (Al), molybdenum (Mo) and Si leading to various intermetallics, following with poor conductivity as open-circuit [48].

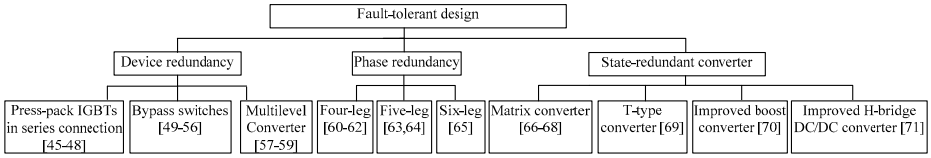

Fig. 4. Classification of typical fault-tolerant circuits.

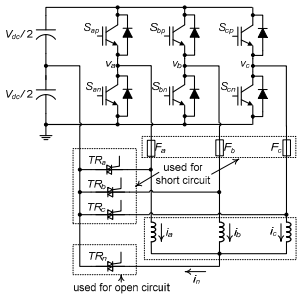

Fig. 5. Typical bypass switches redundant circuit [51].

Another way is using bypass switches, as shown in Fig. 5 [49]. The bypass switches are located between the neutral point and phase output. Failure occurred in switching devices (e.g. S_{ap}) can be cleared by blowing fuses (e.g. F_a) through turning on the bypassing switch (e.g. TR_a). The circuit operates as a four-switch three-phase inverter, with lower quality of the output. This topology can also handle open-phase failure in motor drive application, which needs to turn on TR_n and change the phase currents to maintain motor's torque constant. This method has been applied in neutral point clamped (NPC) converters [50]. Similar solutions are also presented in [51-56].

The other method with both series redundancy and bypass switches is cascaded H-bridge multilevel (CHBM) converter [57,58] or modular multilevel converter (MMC) [59]. When a fault occurs to a switch, the faulty H-bridge (or half H-bridge) cell is bypassed. The output voltage magnitude can be maintained with an increase of harmonic distortion.

B. Phase Redundancy

This concept consists of introducing an additional phase leg to replace a faulty phase leg, as shown in Fig. 6 [60]. The fault-tolerant control scheme is as follows: firstly, the gate driving signals of the two switches in the faulty leg (e.g. S_1 and S_2) are set to be zero level; secondly, the suited bidirectional switch is triggered (e.g. t_1); finally, the two switches in redundant phase (e.g. S_7 and S_8) are controlled by gate driving signals to resume the role of the two switches in faulty leg. This method has been applied in three-level converters [61,62]. Five-leg [63,64] and six-leg converter [65] also have similar fault redundancy.

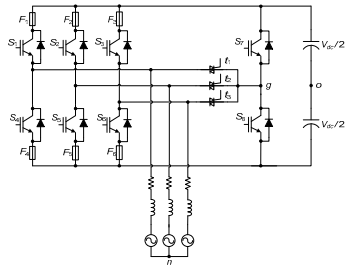

Fig. 6. Typical phase redundant circuit [61].

TABLE II. SUMMARY OF FAULT-TOLERANT CIRCUITS' PERFORMANCE WITH POWER SWITCHES FAILURE

Fault-tolerant Design	Failure Types of Power Switch	
	Short-circuit	***Open-circuit***
Press-pack IGBTs in Series Connection	✓[a]	✗[b]
Bypass Switches	✓[c]	✓
CHBM/MMC	✓	✓
Four-leg Converter	✓	✓
Five-leg Converter	✓	✓
Six-leg Converter	✓	✓
Matrix Converter	✗	✓
T-type Converter	✗	✓
Improved Boost Converter	✗	✓
HBALSC	✓	✓

[a] Maintain Operation with Normal Output; No fault-tolerant ability; Maintain Operation with Degraded Output

C. State-redundant Converter

Some circuits have inherent redundant ability, such as the sparse matrix converter [66-68], and T-type three-level converter [69], which can handle open-circuit failure of switches. Moreover, researchers also proposed modifications to traditional converters to obtain fault-tolerant ability, such as an improved three-level boost converter for photovoltaic applications [70], an H-bridge DC-DC converter with auxiliary leg and selector cells (HBALSC) [71].

A summary of fault-tolerant circuits' performance with respect to power switches failure is presented in Table II. It is worth mentioning that short-circuit failure is more difficult to handle than open circuit, and it usually needs very short detection times.

V. CONCLUSIONS

Catastrophic failure of IGBT is fairly important issues both in design phase and in operation phase of power electronic converters. The failure mechanisms of two open-circuit modes and four short-circuit modes are reviewed in this paper. Even though the initial triggering factors for those failure modes are different, the final destruction is almost due to over-temperature, which reveals the importance of thermal design and fine thermal management of IGBTs in reliability-critical applications. At present, plenty of circuit-level fault-tolerant solutions are available to isolate faulty IGBTs and enhance converter reliability, which have been discussed in this work. Exploration of fault-tolerant solutions with reduced complexity and reduced cost is a hot theme and progresses in this field are highly expected in the near future.

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Publication 5

(*Conference Contribution*)

Fast and Accurate Icepak-PSpice Co-Simulation of IGBTs under Short-Circuit with an Advanced PSpice Model

Wu, Rui; Iannuzzo, Francesco; Wang, Huai; Blaabjerg, Frede

The paper has been published in the
Proceedings of the 7_{th} *IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, pp. 1-5, 2014.

DOI:10.1049/cp.2014.0466

Fast and Accurate Icepak-PSpice Co-Simulation of IGBTs under Short-Circuit with an Advanced PSpice Model

Rui Wu*, Francesco Iannuzzo†, Huai Wang*, Frede Blaabjerg*

**Aalborg University,Denmark,rwu@et.aau.dk, hwa@et.aau.dk, fbl@et.aau.dk, † University of Cassino and southern Lazio,Italy, iannuzzo@unicas.it*

Keywords: Insulated Gate Bipolar Transistor (IGBT), Co-simulation, Short-circuit, Finite-Element Method (FEM), PSpice.

Abstract

A basic problem in the IGBT short-circuit failure mechanism study is to obtain realistic temperature distribution inside the chip, which demands accurate electrical simulation to obtain power loss distribution as well as detailed IGBT geometry and material information. This paper describes an unprecedented fast and accurate approach to electro-thermal simulation of power IGBTs suitable to simulate normal as well as abnormal conditions based on an advanced physics-based PSpice model together with ANSYS/Icepak FEM thermal simulator in a closed loop. Through this approach, significantly faster simulation speed with respect to conventional double-physics simulations, together with very accurate results can be achieved. A case study is given which presents the detailed electrical and thermal simulation results of an IGBT module under short circuit conditions. Furthermore, thermal maps in the case of non-uniform threshold voltage/ solder resistance/ gate resistance among the cells are presented in comparison with the case of uniform distribution, evidencing the capabilities of studying short-circuit of aged devices by the presented technique.

1 Introduction

In modern power electronic systems, one of the challenges is to design robust and reliable power electronic products while avoiding over-sized design margins [1]. Meanwhile, simulation tools have played an important role in researching and optimized designing of power semiconductors and power electronic systems. One of the trends of simulation technologies in power electronics is toward multi-disciplinary design platform which includes electrical, thermal, magnetic and mechanical simulations [2]. For instance, the phenomena of current constriction and thermal runaway, which are responsible for failures of IGBT modules during heavy loads and short circuits, are usually connected with a critically high junction temperature. To well study these issues, a precise electro-thermal simulation is needed to accurately estimate the junction temperature of IGBT modules in order to determine the robustness margins and prevent potential failures with high confidence levels.

There is already plenty of research work on electrical-thermal co-simulation of power electronic devices and packages. C.-H. Lin obtained hot spots caused by high current density crowding in Printed Circuit Board (PCB) packages by using commercial electrical-thermal co-simulating Finite-Element Method (FEM) tools. The difference between co-simulation and infrared camera measurement was less than 10%, however the computing time is not mentioned and could be very slow for a more complicated system, for example power semiconductors [3]. J. Xie and M. Swaminathan utilized a comprehensive finite volume modelling of electric potential distribution equations and heat equations to implement electrical-thermal co-simulations of electronic packages [4]. Similarly, T. Lu and J. Jin improved traditional electrical-thermal FEM co-simulation to gain faster speed of electronic packages (e.g. PCB board) [5]. Proposed co-simulations are aimed at integrated circuit (IC) simulations and optimizations, which are hard to extend to power semiconductor study since advanced electrical model is absent.

Concerning power semiconductor study, some researchers attempted to extend widely-used very accurate electrical simulation tools (e.g. Spice, Saber) to electrical-thermal simulations by introducing lumped thermal impedance, but they cannot provide accurate junction temperature as well as temperature distribution and hot spots in power semiconductors because of the intrinsic limitation of such tools in the number of nodes to few thousands [6-8]. There are also commercial multi-discipline tools, e.g. SystemVision [9], which can connect multiple domain-specific tools (MathWorks Simulink, National Instruments LabVIEW, SystemC, C/C++, Java, and Spice) and processes, together in a single simulation environment, but still lacking of accuracy due to using lumped thermal impedance.

On the other hand, FEM software are very specialized to single physics, e.g. electromagnetic physics, thermal physics, semiconductor physics, etc., but they lack in optimization when a multi-physics approach is used, so that a dramatic worsening in simulation times and sometimes in accuracy is obtained. For instance, thermal simulation with Icepak [10] can be connected to circuit-level simulator Simplorer [11] in ANSYS, but the process is heavy and slow (seconds per simulation point). Besides slowness, a lot of information is unavoidably omitted by this intrinsically-single-cell approximation method, e.g. uneven fast junction temperature variation and hot spots dynamics in the semiconductor chips, which strongly limit the prediction of imbalances among the cells of the real device. This issue becomes even more critical for power semiconductors under abnormal conditions (e.g. short-circuit, overload), where two physics at high accuracy

levels are required. There, it is vital to determine the precise distributed dynamic power density input to thermal FEM simulation. Of course, a compact electrical model can be integrated into FEM thermal simulators [12-13], which can reduce the computing time but also the accuracy. Another way is physical cell-level (i.e. in the scale of few square microns) FEM simulation, like TCAD, which can hardly predict the temperature distribution among several cells [14], which is critical for studying short-circuit behavior, especially for aged device.

A novel perspective could be connecting a physics-based, device-level, distributed electrical simulation tool, to a thermal FEM simulation. This could gain flexibility on the electrical side without losing accuracy on the thermal side. A physics-based IGBT model in PSpice which has shown accurate results, high modularity and fast simulating speed as well is a good candidate to this aim [15].

This paper discusses the aforementioned co-simulation approach to the electro-thermal simulation of power IGBTs adopting the model presented in [15], which is suitable to simulate normal as well as abnormal conditions. Moreover, among other things, one large advantage of such approach is that independent time steps can be adopted for the electrical and thermal parts, thus gaining huge calculation efficiency. A case study is given which will present the detailed electrical and thermal simulation results of an IGBT module under short circuit conditions based on such advanced PSpice model. Furthermore, thermal maps in the case of non-uniform threshold voltage/solder contact resistance/ gate resistance among the cells have been achieved together with the case of uniform distribution, evidencing the new approach's capabilities of studying the impact of variations of geometry and electrical parameters due to manufacturing process and/or material degradation on short-circuit in aged devices.

2 IGBT electro-thermal simulation setup

The proposed electro-thermal co-simulation method includes three major parts: IGBT electrical model in PSpice, IGBT thermal analysis model in ANSYS/Icepak, and a monitoring program in MATLAB. Based on the electrical simulation, a map of power loss distribution inside the chip is obtained and sent to the ANSYS thermal simulation, then ANSYS/Icepak thermal simulation feeds back the temperature distribution to the PSpice electrical simulation, so finally the chip temperature distribution can be achieved. The simulation setup structure is shown in Fig. 1, whose details will be illustrated as follows.

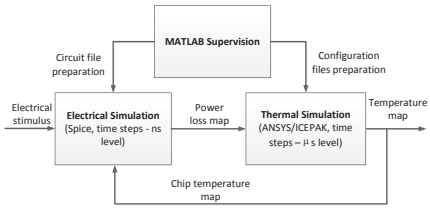


Fig. 1. Structure of the proposal simulation setup

2.1 PSpice model preparation

The physics-based lumped charge IGBT model proposed in [15] shows more accurate results and comparable simulation speed for high voltage IGBTs than the PSpice IGBT native model. Here its operating principle is briefly described. The basic idea is subdividing the device into a few regions characterized by constant doping and/or carrier lifetime, and the behaviour of each region is described by means of few lumped charges placed in proper aggregation points, which is shown in Fig. 2, resulting in a very compact model.

In such model, few parameters must be identified [15]: chip area, transconductance, stray resistance, stray inductance, and gate capacitances, most of them directly obtainable from the datasheet. In the co-simulation, the IGBT chip is simulated as a PSpice circuit containing an arbitrary number of cells, each of whose is a model like the one of Fig. 2, whose area is opportunely scaled.

2.2 Icepak model preparation

A detailed Icepak geometry model is necessary for thermal simulation. In the case study, the geometry of the considered setup is shown in Fig. 3(a), and the cross section in the vertical plane is shown in Fig. 3(b): one 12.5mm wide square IGBT chip and one 9mm wide square diode chip are mounted together in a module, whose ratings are 1700V/25A. Apart from the chips, the module consists of standard DCB sections soldered to a Cu baseplate.

All geometry and material information are included in the Icepak "model" file, in which the power loss information is blank and will be updated by the PSpice simulation later. All thermal simulation setting information are included in the Icepak "problem" file, in which the monitoring points,

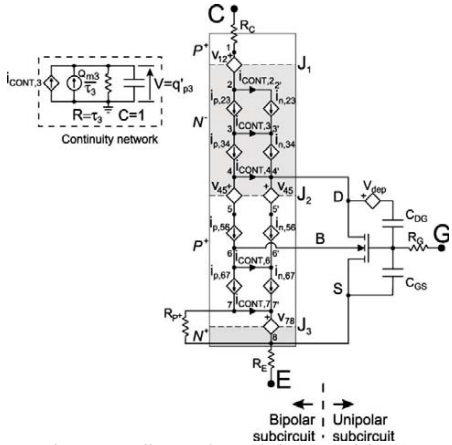
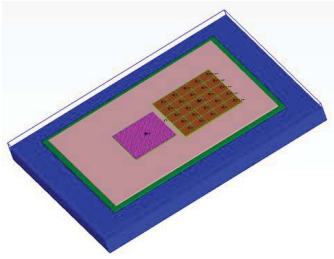
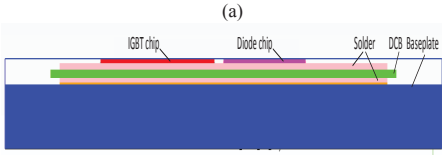


Fig. 2. Overall IGBT lumped charge model [15].



(a)



(b)

Fig. 3. (a) Geometry of the considered setup; (b) details of the cross section on the vertical plane

together with simulation step and end times are defined.

2.3 MATLAB co-simulation script

The presented approach is implemented as a Matlab script which coordinates the above two software at each thermal simulation step. Operations are divided in preparation time and simulation time.

At the preparation time, the Matlab script automatically divides the device under test (i.e. the IGBT) in an arbitrary number of virtual cells. The only condition required is that it should be rectangle-shaped. In the study case, a 5-by-5 array of cells has been adopted (see Fig. 3.a). Cells include power sources placed on a layer at the surface of the IGBT chip. One PSpice subcircuit is automatically generated for each cell

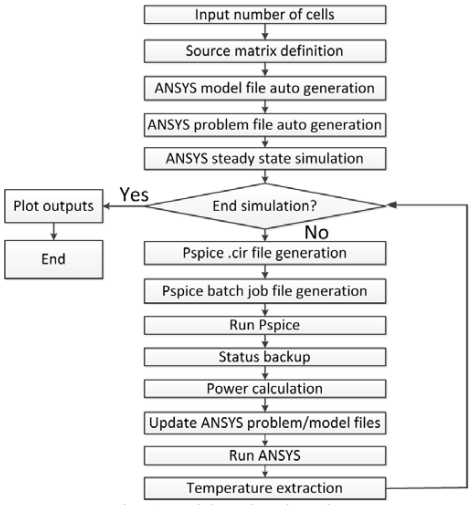


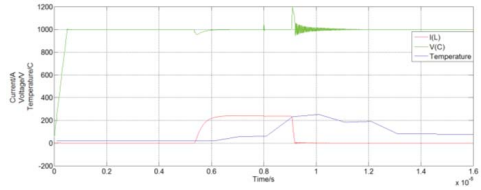
Fig. 4. Matlab Script Flow chart.

starting from a circuit template file, that includes the parameter identified for the considered device, and all of them are connected in parallel. The user-defined external PSpice circuit provides the required electrical stimuli.

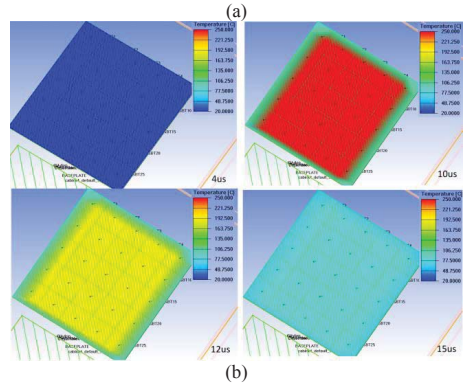
At the simulation time, power loss of each cell is calculated by the PSpice circuit with arbitrary time accuracy (typically nanoseconds) for a given constant temperature map. The Pspice simulation lasts a thermal time step (typically in the range of microseconds) and it is stopped. At this point, dissipated power losses are given to the thermal block – the "model" and "problem" files in Icepak are updated accordingly, and the thermal simulation in Icepak is run. Afterwards, temperatures are input back to the PSpice model and so forth. This process is illustrated in Fig. 4 and continues until the end of simulation.

3 Results and discussion

In the case study we propose, the setup shown in Fig. 3 is subject to several short circuit tests. The IGBT chip is divided into 5 by 5 cells, and the typical simulation duration is 16 µs, including 8 steps, 2 µs each. It is worth to note that the diode does not operate in this case. Short-circuit happens at 5 µs, and ends at 9 µs. Each step takes around 90 s to be evaluated (12 minutes in total for 4*i7 cores@ 2.6Ghz, 4Gb RAM DDR3), including automatic power loss loading, thermal initial condition setting, Icepak thermal simulation, temperature data saving, cell temperature loading, electrical



(a)



(b)

Fig. 5. (a) Short-circuit current/voltage PSPICE waveforms; (b) IGBT chip temperature map in ICEPAK during short-circuit at 4/10/12/15 µs (times bottom right of each image)

initial condition setting, PSpice simulation and power loss data saving.

3.1 Balanced short-circuit simulation

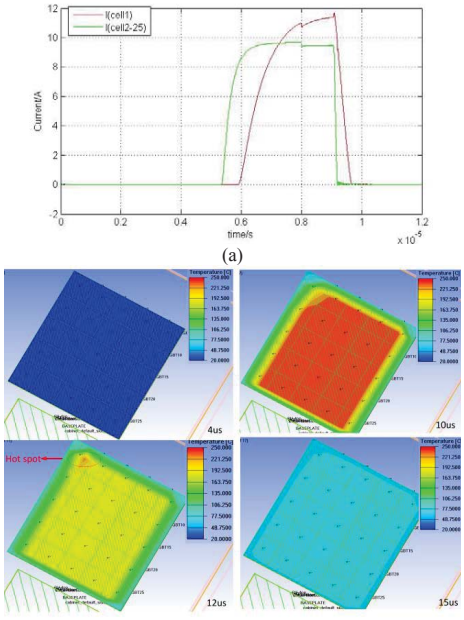
When short-circuit happens during IGBT turn-on (at time=5µs), collector current Ic rises rapidly until reaching saturated value - 230A, as shown in Fig. 5(a). On the same picture the simulated temperature is reported. As the reader can see, sampling time has been arbitrary set to 1us, and IGBT chip's temperature rise as high as 250°C at 10 µs. After the short-circuit turn-off, the chip temperature falls to normal value again. Temperature rises and falls uniformly on the whole chip but the periphery, where cells are cooler than the central ones.

3.2 Short-circuit simulation on imbalanced Vth

As announced before, the proposed electro-thermal co-simulation method has been used to simulate imbalances among the cells in the chip. In fact, due to aging and/or stresses in the real lifetime of the module, degradations and deviations of electrical parameters (e.g. collector resistance Rc, gate resistance Rg, and threshold voltage Vth) are common among the several cells inside the IGBT chip.
A case study of imbalance in Vth is here given. In the PSpice model, the upper-left-corner cell Vth is lower than the other cells, which leads to the imbalanced short-circuit current as shown in Fig. 6(a).
Between 10 µs and 11 µs, a hot spot formation is evidenced by the temperature rising back, as shown in Fig. 6(b). This is confirmed by Fig. 6(a), where the current of the sole cell increases without control up to the turn off time.

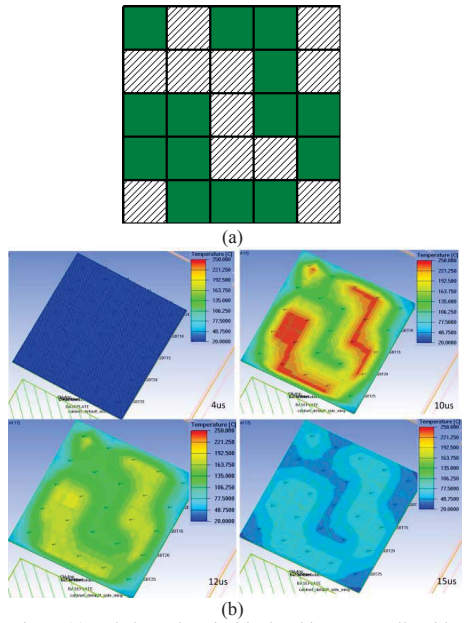
3.3 Short-circuit simulation on imbalanced Rc

In the real lifetime of IGBT module, the solder degradation will unavoidably happen to some parts of the chip. Consequently, there will be imbalanced Rc inside the chip. The proposed electro-thermal co-simulation supplies capability to analyse the impact of this material degradation.
A case study is here given. In Fig. 7(a) the green cells are characterized by higher Rc than the other cells, in order to simulate contact degradation of such cells. Poor contacts lead to the higher Rc and lower current, therefore to imbalanced short-circuit current densities. During the short-circuit, the unequal temperature distribution is effectively predicted, as shown in Fig. 7(b).



(a)
(b)

Fig. 6. (a) Unbalanced short-circuit current in PSPICE; (b) IGBT chip temperature map due to unbalanced Vth at 4/10/12/15 µs (times bottom right of each image)



(a)
(b)

Fig. 7. (a) Unbalanced Rc inside the chip, green cells with normal contacts, hatched are degraded cells; (b) IGBT chip temperature map due to unbalanced Rc at 4/10/12/15 µs (times bottom right of each image)

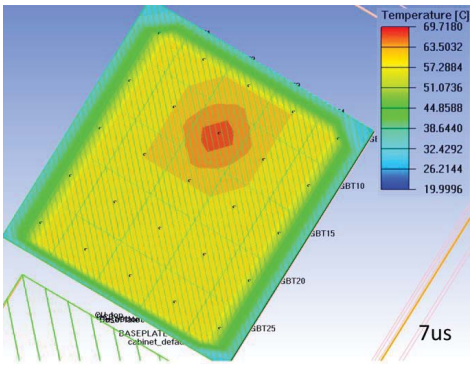


Fig. 8. Unbalanced Rg leads to IGBT chip temperature map during short-circuit turn-on at 7 µs

3.4 Short-circuit simulation on imbalanced Rg

The proposed electro-thermal co-simulation also supplies capability to analyse the impact of variations of geometry parameters, for example the imbalanced Rg due to location. In this latter case study, the cell under the gate bond wire has much smaller gate resistance, which leads to faster turn-on than the other cells. Consequently, a hot spot during turn-on is correctly predicted, as shown in Fig. 8, although it doesn't lead to instability.

4 Conclusions

A new approach involving ANSYS/Icepak and an advanced IGBT PSpice model has been presented, that exhibits an unprecedented compromise between accuracy of results and simulation speed. The approach successfully predicts abnormal operating conditions like hot spots due to variations of the electrical and geometrical parameters among the device cells, for example threshold voltage and solder resistance.

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Publication 6

(*Conference Contribution*)

Electro-thermal Modeling of High Power IGBT Module Short-circuits with Experimental Validation

Wu, Rui; Iannuzzo, Francesco; Wang, Huai; Blaabjerg, Frede

The paper has been published in the
Proceedings of the 2015 Annual Reliability and Maintainability Symposium (RAMS),
pp. 1-7, 2015.

DOI:10.1109/RAMS.2015.7105151

Electro-Thermal Modeling of High Power IGBT Module Short-Circuits with Experimental Validation

Rui Wu, PhD student, Aalborg University, Denmark
Francesco Iannuzzo, Professor, Aalborg University, Denmark
Huai Wang, Assistant Professor, Aalborg University, Denmark
Frede Blaabjerg, Professor, Aalborg University, Denmark

Key Words: Insulated Gate Bipolar Transistor (IGBT), Short-circuit, Electro-Thermal Model, Power Module

SUMMARY & CONCLUSIONS

A novel Insulated Gate Bipolar Transistor (IGBT) electro-thermal modeling approach involving PSpice and ANSYS/Icepak with both high accuracy and simulation speed has been presented to study short-circuit of a 1.7 kV/1 kA commercial IGBT module. The approach successfully predicts the current and temperature distribution inside the chip of power IGBT modules. The simulation result is further validated using a 6 kA/1.1 kV non-destructive tester. The experimental validation demonstrates the modeling approach's capability for reliable design of high power IGBT power modules given electrical/thermal behavior under severe conditions.

1 INTRODUCTION

Power electronic systems play a particularly important role in motor drives, utility interfaces with renewable energy sources, power transmission, electric or hybrid electric vehicles and many other applications. In 2012, nearly 70% of all electricity was processed through power electronics, the rate of which is likely to reach 80 % in 2015 [1]. In modern power electronic systems, there are increasing demands to improve whole system endurance and safety level while reducing manufacturing and maintenance costs [2]. According to manufacturers' questionnaires, semiconductor devices are considered the most critical and fragile component in industrial power electronic systems [3], the failure of which result in up to 34% of power electronic system failures [4]. Because IGBTs are one of the most critical components as well as the most widely used semiconductor devices in industrial power electronic systems in the range above 1kV and 1kW [4], the reliability of IGBTs has drawn more and more attention. In particular, the ability to withstand abnormal conditions (e.g. short-circuits), is strictly required to achieve sufficient robustness in critical applications, especially where the maintenance costs are very high [5].

It is worth pointing out the junction temperature (Tj) is probably the most critical parameter responsible for IGBT converters failures. For instance, the phenomena of current constriction and thermal runaway, which cause IGBT modules failures during heavy loads and short-circuits, are commonly connected with regenerative effects involving high Tj [6]. Additionally, the final destruction coming from various failure-triggering events, (e.g. dynamic breakdown, latch-up and gate driver failure) is similarly due to high Tj [7]. Therefore, a precise electro-thermal model is required to accurately estimate the Tj in order to determine IGBT modules robustness margins and prevent potential failures with high confidence levels.

Plenty of research has been conducted into IGBT electrical-thermal co-simulation. Traditional ways of extending widely-used electrical simulation tools (e.g. Spice, Saber) to electrical-thermal simulations by introducing lumped thermal impedance, cannot provide accurate Tj as well as temperature distribution and hot spots because there are only a few thousands intrinsic nodes in such tools, which are not enough to guarantee the accuracy [8]. Finite-Element Method (FEM) software lacks optimization with respect to a multi-physics approach, resulting in a dramatic degeneration in simulation speed and accuracy. For instance, thermal simulator Icepak connected with circuit-level simulator Simplorer in ANSYS leads to heavy and slow process (seconds per simulation point). Moreover, this intrinsically-single-cell approximation method unavoidably loses plenty of information, e.g. uneven fast Tj variation and hot spots dynamics in IGBT chips, which strongly limit the prediction of imbalances among the cells of the real device. Another solution - physical cell-level (i.e. in the scale of few square microns) FEM simulation, like TCAD, can hardly predict temperature distribution among several cells [9], which is critical for studying short-circuit behavior.

Recently, a novel electro-thermal modeling method has been proposed, which combines a physics-based, device-level, distributed electrical PSpice model with a thermal FEM simulation, gaining flexibility on the electrical side without losing accuracy on the thermal side. Moreover, independent time steps are adopted for the electrical and thermal parts, thus achieving high calculation efficiency [10], [11]. This paper applies this method to model a 1.7 kV/1 kA IGBT power

978-1-4799-6703-2/15/$31.00©2015 IEEE

module, and further study its electrical/ thermal behavior during short-circuits. The electro-thermal model is further validated by a 6 kA/1.1 kV Non-Destructive-Tester (NDT) for IGBT short-circuit tests. The paper is organized as follows: Section II introduces the basic principle of the novel electro-thermal modeling method. Then it presents the case study of a 1.7 kV/1 kA IGBT power module, to further describe the procedures, including profile definition, supervision scripts and model preparation. Section III shows the simulation results. It demonstrates the capability of the proposed method to investigate the electrical/ thermal behaviors during the power modules short-circuit, especially the electro-thermal interacting effects. Section IV briefly introduces the NDT setup, including short-circuit time setting schemes. Section V compares the modeling results with experimental results, demonstrating the new approach's accuracy and capabilities. Section V concludes the paper with discussions.

2 *ELECTRO-THERMAL MODELING OF HIGH POWER IGBT MODULE*

The basic principle of the proposed electro-thermal modeling method is described in this section. In order to illustrate this novel PSpice-Icepak co-simulation method, a case study of a 1.7 kV/1 kA commercial IGBT module is given in this section. The IGBT power module information is introduced. Then, the co-simulation configuration is explained in details, including: simulation profile definition, electrical model and thermal model configurations, as well as MATLAB supervision configuration.

2.1 *Basic Principle*

The proposed electro-thermal modeling method includes three major parts: a physics-based, device-level IGBT electrical model in PSpice, IGBT thermal analysis model in ANSYS/Icepak, and a monitoring program in MATLAB.

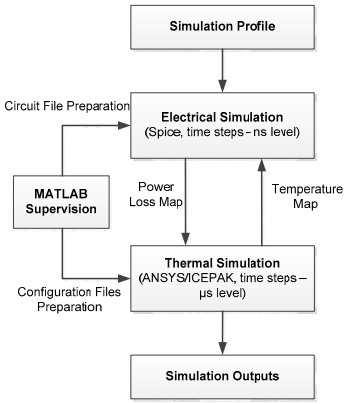


Fig. 1. Structure of the proposed electrical-thermal modeling method.

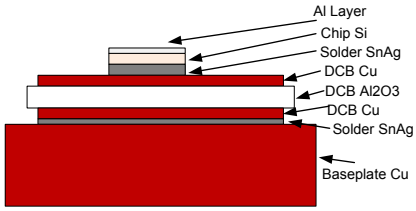


Fig. 2. Schematic typical cross-section of the multilayers in IGBT power modules.

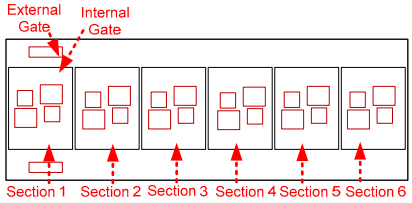


Fig. 3. Geometry of the internal structure of studied 1.7 kV/1 kA IGBT power modules.

Based on the PSpice electrical simulation, power loss distribution inside the chip is obtained and sent to the thermal simulation, and then ANSYS/Icepak thermal simulation feeds back temperature distribution to the PSpice electrical simulation, finally the chip temperature distribution can be achieved. The co-simulation process is shown in Fig. 1, of which the details will be illustrated in following sections through a case study of a 1.7 kV/1 kA IGBT power module.

2.2 *Information about the Studied IGBT Module*

This 1.7 kV/1 kA IGBT power module is widely used in high power applications, for instance wind turbine systems. The main specifications of the IGBT module are shown in Table I. The chips are soldered on a standard Direct Copper Bonded (DCB) layer, which is further soldered to a Cu baseplate, and the cross section structure is plotted in Fig. 2. It is worth noting there are six identical sections connected in parallel to increase the current capability, as shown in Fig. 3, so that the rated short-circuit current is 4 kA. Each section includes two IGBT chips and two freewheeling diode chips, which are configured as a half-bridge.

Characteristic	Value
Collector-emitter voltage V_{CES}	1.7 kV
Continuous DC collector current I_{Cnom}	1 kA
Rated short-circuit current I_{SC}	4 kA
Gate-emitter maximum voltage V_{GES}	+/- 20V
Number of parallel sections	6

Table 1 –The studied IGBT power module main specifications.

2.3 *Simulation Profile Definition*

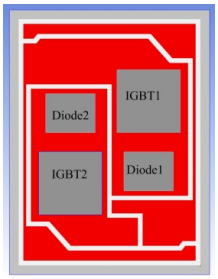
As is well known, the most critical abnormal working

condition for IGBTs is short-circuit, where both high voltage and high current are applied to the device at the same time. Therefore, a standard 10 µs short-circuit duration is chosen in the case study, with a thermal simulation step of 1 µs. It is worth noting that the diodes do not operate in this case study.

A MATLAB script is implemented to prepare configuration files and then coordinate information sharing between the other software at each thermal simulation step. Operations are divided into preparation state and simulation state.

During the preparation state, the MATLAB script automatically divides the device under simulation (i.e. the IGBT) into a specific number of virtual cells, which should be rectangle-shaped. Each cell includes one power source and one temperature monitoring point, which are placed in the IGBT body. One PSpice sub-circuit is automatically generated for each cell starting from a circuit template file, that includes the parameter identified for the considered device, and all of them are connected in parallel. The user should also define the external PSpice circuit profile as normal operation, overload or short-circuit.

During the simulation state, the power loss of each cell is calculated by the PSpice circuit with time resolution of nanoseconds for a given constant temperature map. The PSpice simulation lasts a thermal time step (typically in the range of microseconds) and it is stopped. At this point, dissipated power losses are given to the thermal simulation – the corresponding files in Icepak are updated accordingly, and the thermal simulation in Icepak is then done. Afterwards, the temperature data are transferred back to the PSpice model and so forth.



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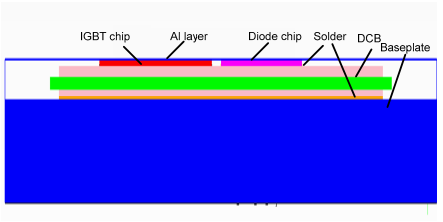


(b)

Fig. 4. IGBT thermal model constructed in Icepak: (a). geometry of one section of IGBT power module, (b) details of the cross section on the vertical plane.

In the electrical model, the studied IGBT chip is divided into 4 by 4 cells. According to the information from manufacturer, the IGBT module's stray inductance is 10 nH, its gate capacitance is 81 nF, while the IGBT chip is 12.6 mm by 12.6 mm square size. Based on the datasheet information, corresponding IGBT lumped charge model can be obtained according to the method in [12].

Based on the information provided by the IGBT manufacturer, one IGBT section model is constructed in Icepak for thermal simulation. The geometry information of one section in Icepak is shown in Fig. 4 (a), and the cross section of the Icepak model is shown in Fig. 4 (b). It contains Al top layer, IGBT trench gate layer, IGBT body layer, solder, DCB and baseplate. Power source is located in the IGBT body layer. 543,000 nodes are defined in Icepak model. The thermal conductivity and heat capacity information of the materials used in the simulations at 25 ºC are listed in Table 2.

Material	Thermal Conductivity (W/m-K)	Heat Capacity (J/Kg-K)
Aluminum	237	897
Silicon	148	705
Solder	57	220
Copper	401	385

Table 2 – IGBT power module material thermal properties at 25 ºC [13].

3 ELECTRO-THERMAL SIMULATION RESULTS

As mentioned in last section, a standard 10 µs short-circuit duration has been chosen in the case study. There are two different short-circuit types: Type 1 short-circuit happens during IGBT turn-on, while Type 2 short-circuit happens when IGBT is at on-state, as illustrated in Fig. 5. At present, only type 1 short-circuits are studied in this paper.

3.1 *Electrical Simulation Results*

When a short-circuit happens during IGBT turn-on (at 5 µs), collector current Ic rises rapidly until reaching the saturated value of 780 A. It is noted that the IGBT chip's rated current is 150 A. Due to the high current slope di/dt and the stray inductance, there is a voltage drop during the short-circuit turn-on, at the collector voltage waveform. The PSpice simulation results are plotted in Fig. 6.

According to semiconductor physics, IGBT short-circuit current decreases with the junction temperature rising [14]. This phenomenon is also evidenced in the simulation, as shown in Fig. 6. Because the IGBT cells temperature is updated every thermal step – 1 µs, the short-circuit current also decreases by 1 µs step. As introduced in Section II, part 3, the thermal step duration can be modified in the MATLAB script according to requirements.

The voltage overshoot during the short-circuit turn-off is also because of the high current slope di/dt and the stray

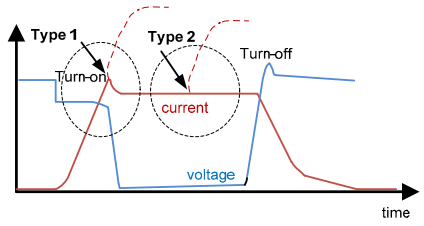


Fig. 5. Two types of short-circuits: Type 1 occurs during turn-on, Type 2 occurs during conduction state.

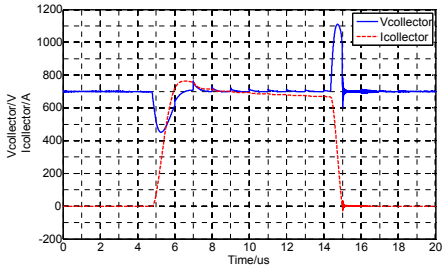


Fig. 6. PSpice simulated short-circuit current/voltage waveforms of the IGBT chip.

inductance.

3.2 *Thermal Simulation Results*

Four chip temperature maps obtained during short-circuit are depicted in Fig. 7. They are before short-circuit (at 2 µs), during short-circuit (at 10 µs), after short-circuit (at 16 µs and 18 µs) respectively. In the study case, temperature rises almost uniformly on the whole chip, but still some differences can be observed. This is because of the not perfectly equal current distribution among cells. The cells under bond-wires are conducting more currents than the others.

Before short-circuit, the chip is at room temperature (25 ºC) (as shown in the first picture at 2 µs). During short-circuit (at 10 µs): cells under bond wires (cells 1-4 and cells 9-12) are about 5 ºC hotter than other ones because of the imbalanced current. After the turn-off of short-circuit, the temperature keeps rising due to the heat flow from the Si layer. IGBT chip's temperature rises as high as 150 °C at 18 µs due to the high energy shock in these conditions.

4 EXPERIMAL VALIDATION BY MEANS OF NON-DESTRUCTIVE TESTING SETUP

4.1 *Testing Setup Structure and Principle*

The most critical abnormal working condition for IGBTs is a short-circuit, where both high voltage and high current can

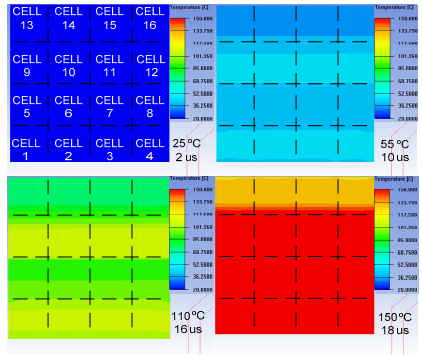


Fig. 7. IGBT power module chip temperature map in Icepak during short-circuit at 2/10/16/18 µs (times and highest temperature at bottom right of each image) (Temperature color bar – max 150 ºC, min 20 ºC).

damage the device within several tens of µs. In order to test short-circuits without damage, a non-destructive testing method has been proposed, the circuit of which is shown in Fig. 8. The NDT includes the Device Under Test (DUT), the series protection, parallel protection, load inductance L_{load}, DC link capacitance C_{DC}, a high voltage power supply V_{DC}, Schottky diodes, negative-voltage capacitance C_{NEG} with corresponding negative voltage supply V_{NEG}.

The NDT structure includes the following parts. A high-voltage power supply charges up a high-voltage capacitor bank C_{DC}. The stored energy is used to supply power for short-circuits. The on-state series protection switch will be switched off immediately after the test and save the DUT. A Computer-Aided-Design (CAD) busbar has been developed to minimize the overall circuit inductance by optimization of the mutual coupling of the busbar components [15]. A 100 MHz FPGA provides the driving signals for the DUT and the switches for the protection, and also provides the precise time control for electrical measurement. The remote control and data acquisition is achieved by a Personal Computer (PC) which supervises the operation by connecting a LeCroy HDO6054-MS oscilloscope via an Ethernet link and a FPGA board through an RS-232 bus. Two commercial IGBT drivers

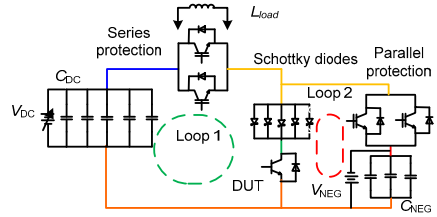


Fig. 8. Detailed schematic of the power circuit of the Non-Destructive Tester.

drive the protection switches and the DUT respectively. In order to perform short-circuits, the corresponding protection circuit on the DUT drivers has been deactivated. During tests, collector current, collector voltage and gate voltage waveforms are acquired together with the current flowing through a specific section of the DUT.

The operating principle is as follows: as shown in Fig. 8, the power circuit is divided into two loops –Loop 1, (the main loop) including the series protection, and Loop 2, including a parallel protection; the DUT is located in the common branch. The tester is operated in a standard single-shot way, so that the energy stored in the capacitors C_{DC} is used for the tests. C_{DC} and C_{NEG} are composed of five and three capacitors in parallel, respectively, in order to reduce the intrinsic stray inductances. The same principle has been adopted for the two switches of the series protection, the two switches of the parallel protection and the five Schottky diodes.

Loop 2 is designed to improve the performance of the NDT. The "non-destructive testing" means that the series protection is activated right after the commutation to prevent the DUT from explosions in case of failure. This capability is strictly dependent on the series protection's capability to cut the current flowing through the DUT to zero immediately after the test. However, the turn-off transition of the series protection is non-ideal because IGBT switches have current tails, which would continue flowing through the DUT. To avoid this effect and divert the current tail, the parallel protection is fired up together with the activation of the series one. As demonstrated in [16], to improve the parallel intervention as well, a negative voltage biases a capacitor bank C_{NEG} in order to enhance the voltage fall promptness during IGBT turn-on. Furthermore, to avoid a negative current flowing through the DUT, the Schottky diode bank is placed in series.

4.2 *Short-circuit Operation Time Setting*

The NDT can provide both short-circuit types by different configuration and control time schemes. At present, only type 1 short-circuits are studied. The circuit configuration and the control timing scheme for type 1 short-circuits are illustrated as follows:

Type 1 short-circuits happen at the device turn-on transient. The load inductance L_{load} is removed in the main circuit. Before tests, the series protection is in on-state and the parallel protection is in off-state. Loop 1 has the stray inductance only and the Schottky diodes behave almost ideally, so the DUT is connected directly to the C_{DC} capacitors. During the tests, the DUT falls to short-circuit when it is triggered. After the precise controlled time by 100 MHz FPGA, the DUT short-circuit is switched off by series protection IGBTs. At the same time, the parallel protection is turned on to avoid the undesirable tail current through DUT. The corresponding control time sequences of the series and parallel protections and DUT are as shown in Fig. 9. The negative voltage V_{NEG} can speed up the parallel protection, and the Schottky diodes can avoid a current flow from the DUT to the negative voltage.

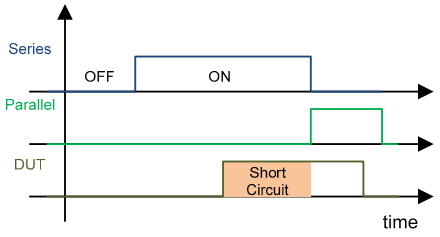
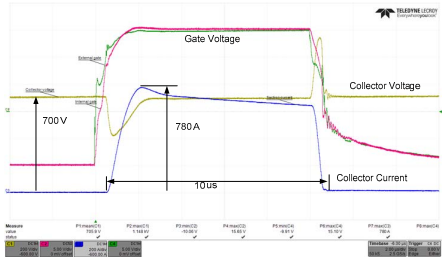


Fig. 9. Control timing settings of all the power devices for Type 1 short-circuit.

4.3 *Experimental Validation*

In order to validate the electro-thermal model of the power module, the short-circuit tests have been carried out at the same condition of the simulation. A 10 μs short-circuit test at 700 V for the studied power module has been performed in the laboratory at room temperature (25 ºC). The short-circuit current of one IGBT chip reaches 780 A, and



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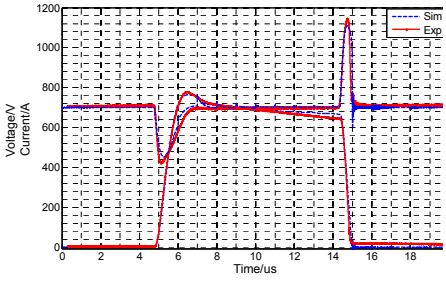

(b)

Fig. 10. (a). Experimental collector voltage and current waveforms during a 700 V/10 us short-circuit for the IGBT module at room temperature 25 ºC, (b). comparison between the simulated short-circuit current and the experimental one under the same condition.

decrease as the time increasing. Experimental collector voltage/ current waveforms are shown in Fig. 10(a). Due to the test circuit stray inductance, it is observed the collector voltage undershoot and overshoot at the starting and end of the short-circuit operation, respectively.

The comparison between the simulated and experimental short-circuit waveforms is shown in Fig. 10(b). It shows that the co-simulation can predict short-circuit current precisely; especially how short-circuit current decreases due to self-heating effects.

CONCLUSIONS

An advanced IGBT electro-thermal modeling approach has been presented to study short-circuits of a 1.7 kV/1 kA commercial IGBT module. The approach successfully predicts the current and temperature distribution inside the chip of power IGBT modules, which is further validated by a 6 kA/1.1 kV non-destructive tester. The experimental validation demonstrated the modeling approach's capability for assisting in reliability design of high power IGBT power modules with respect to electrical/thermal behavior under severe conditions.

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BIOGRAPHIES

Rui Wu, PhD student
Department of Energy Technology, Aalborg University
Pontoppidanstraede 101, 9220 Aalborg East, Denmark

e-mail: rwu@et.aau.dk

Rui Wu received the B.Sc. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2009 and M.Sc. in Power Electronics from China Electric Power Research Institute, Beijing, China in 2012 respectively. He was also employed at China Electric Power Research Institute in 2012. He is currently working toward the Ph.D. degree in Aalborg University, Denmark. His research interests are multi-physics modeling of power devices and power device's behavior during abnormal conditions, especially short-circuits.

Francesco Iannuzzo, Professor
Department of Energy Technology, Aalborg University
Pontoppidanstraede 101, 9220 Aalborg East, Denmark

e-mail: fia@et.aau.dk

Francesco Iannuzzo earned his Ph.D. degree in Electronics and Information Engineering from the University of Naples, Italy, in 2001, with a study on the reliability of power MOSFETs during diode operations. He is primarily specialized in the field of power device modelling.

He is full professor of Reliable Power Electronics at the Aalborg University, Denmark, where he is also part of CORPE (Center of Reliable Power Electronics http://www.corpe.et.aau.dk). He is author or co-author of more than 90 publications on journals and international conferences. His research interests are in the field of reliability of power devices, including against cosmic rays, power device failure modelling and development of non-destructive testing facilities for assessment of MW-scale power modules under extreme conditions.

Prof. Iannuzzo is a senior member of the IEEE (Reliability Society and Industrial Electronic Society) and of AEIT (Italian Electric, Electronic and Telecommunication Association).

Huai Wang, Assistant Professor
Department of Energy Technology, Aalborg University
Pontoppidanstraede 101, 9220 Aalborg East, Denmark

e-mail: hwa@et.aau.dk

Huai Wang received the B.Eng. degree in Electrical and Electronic Engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2007, and the Ph.D. degree in Electronic Engineering from the City University of Hong Kong, Kowloon, Hong Kong, in 2012.

He has been with Aalborg University, Aalborg, Denmark, since 2012, where he is currently an Assistant Professor with the Department of Energy Technology. He is a Visiting Scientist with the ETH Zurich, Zurich, Switzerland, from August to September, 2014 and with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, from September to November, 2013. He was with the ABB Corporate Research Center, Baden, Switzerland, in 2009. He has contributed over 20 journal papers and filed four patents. His current research interests include the reliability of DC-link and AC filter capacitors, reliability of power electronic systems, high voltage DC-DC power converters, time-domain control of converters, and passive components reduction technologies.

Dr. Wang is a recipient of the five paper awards and project awards from industry, IEEE, and the Hong Kong Institution of Engineers. He serves the Guest Associate Editor of the IEEE Transactions on Power Electronics Special Issue on Robust Design and Reliability in Power Electronics, and a Session Chair of various conferences in power electronics.

Frede Blaabjerg, Professor
Department of Energy Technology, Aalborg University
Pontoppidanstraede 101, 9220 Aalborg East, Denmark

e-mail: fbl@et.aau.dk

Frede Blaabjerg was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he was a Ph.D. Student with Aalborg University, Aalborg, Denmark. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives.

He has received 15 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011.

Publication 7

(*Conference Contribution*)

A Comprehensive Investigation on the Short Circuit Performance of MW-level IGBT Power Modules

Wu, Rui; Reigosa, Paula Diaz; Iannuzzo, Francesco; Wang, Huai; Blaabjerg, Frede

The paper has been published in the
Proceedings of 17_{th} *European Conference on Power Electronics and Applications*,
pp. 1-7, 2015.

DOI:

A Comprehensive Investigation on the Short Circuit Performance of MW-level IGBT Power Modules

Rui Wu, Paula Diaz Reigosa, Francesco Iannuzzo, Huai Wang, Frede Blaabjerg
Aalborg University
Pontoppidanstraede 101
Aalborg, Denmark
E-Mail: rwu@et.aau.dk
URL: http://www.en.aau.dk/

Acknowledgements

This work is conducted under the Center of Reliable Power Electronics (CORPE) project framework at Aalborg University, Denmark.

Keywords

«Insulated-Gate Bipolar Transistor (IGBT)», «Power Modules», «Short Circuit», «Current Distribution».

Abstract

This paper investigates the short circuit performance of commercial 1.7 kV / 1 kA IGBT power modules by means of a 6 kA Non-Destructive-Tester. A mismatched current distribution among the parallel chips has been observed, which can reduce the short circuit capability of the IGBT power module under short circuit conditions. Further Spice simulations reveal that the stray parameters inside the module play an important role in contributing to such a phenomenon.

1. Introduction

Nowadays, there are increasingly demands to improve the durability and reliability of modern power electronic systems while reducing the manufacturing and maintenance costs. In order to fulfill these requirements, it becomes more and more important to improve the performance of power semiconductor modules in terms of reduced failure under abnormal conditions [1]. According to the questionnaires surveyed in [2-3], 34% of the manufacturers consider power semiconductor discrete devices or modules as the most fragile components in power electronic systems. Insulated Gate Bipolar Transistors (IGBTs) are the most widely used reliability-critical power devices in industrial power electronic systems in the range above 1 kV and tens of kW, for instance wind turbine systems [4-5]. In medium- and high-power applications with IGBTs, the power module is the most used semiconductor packaging, which usually contains multiple chips connected in parallel to increase its current ratings [6]. IGBT modules usually come with a specified short circuit operation capability of a few μs (e.g., typically 10 μs). However, this allowable short circuit operation duration might be reduced if imbalanced current distribution exists among the multiple chips in IGBT modules. The aim of this paper is to comprehensively investigate the current distribution of IGBT chips of MW-level power modules during short circuit operation.

Because of the variations in chip characteristics and the layout design of each section in the power modules [6], it is difficult to ensure that the currents among the paralleled IGBT chips are identical. This challenge becomes even more critical for the MW-scale IGBT modules, due to the high current ratings (typically kA-level) and the asymmetric geometry. Several researchers have investigated the current sharing under normal operations: in [7-8], the Partial Element Equivalent Circuit (PEEC) method has been applied to analyze the current imbalance of IGBT modules with 2 or 4 chips connected in parallel, while convincing experimental validations are still missing; in [9], the field analysis has been applied to investigate the current imbalance among 6 chips based on the detailed structure. A study on medium power modules (e.g., with a rating of 600 V/300 A) shows that the stray parameters can affect the power loss and temperature distribution among IGBT chips [10], which leads to mismatched lifetimes. This effect becomes even more critical for the short circuit operations, since the current is several times higher than the normal operation values. Some of the chips may withstand higher stresses during short circuits, and therefore fail faster than others in the same power module.

This paper investigates the current imbalance among parallel chips during turn-on short circuit of MW-level IGBT power modules by means of a 6 kA Non-Destructive-Tester (NDT). Based on the experiments on the 1.7 kV / 1 kA IGBT power modules, the most stressed IGBT chips are identified according to the power loss distribution. Moreover, the impact of stray resistances and stray inductances of the IGBT module layouts is studied by Q3D and Spice simulations. This presented findings could be helpful for both the packaging designers and application engineers to optimize the internal layout design, to improve the thermal performance, and finally to enhance the reliability level of IGBT power modules.

2. Specifications of the Device under Test

The experimental study has been carried on a commercial 1.7 kV/1 kA IGBT module. This MW-level module is widely used in wind turbine systems, motor drives and other high power converters. The maximum operating junction temperature is 150 ºC. The rated short circuit current is 4 kA for a gate pulse duration no longer than 10 µs under a maximum DC voltage of 1 kV and an external circuit stray inductance of 30 nH. The main specifications are summarized in Table I.

An outline picture of the Device under Test (DUT) is shown in Fig. 1(a). The package size of the module is 234 mm by 89 mm by 38 mm. There are two power terminals for the DC+ connections (upper IGBT collector), two power terminals for the DC- connection (lower IGBT emitter), and one terminal with two screw connections for the output phase. The upper IGBT gate terminals are on the right side in Fig. 1(a), and the lower IGBT gate terminals are on the left side, which are also aligned with the Negative Temperature Coefficient (NTC) thermistor connections. There are six sections connected in parallel to achieve the rated current of 1 kA. For the sake of clarification, the definition of section numbers is shown in Fig. 1(b): the nearest section to the gate terminals is defined as section 1 and the farthest one is defined as section 6. Each section contains two IGBT chips and two freewheeling diode chips, which are configured as a phase leg.

Table I: The main specifications of the DUT.

Specifications	**Values**
Collector-emitter voltage, V_{CES}	1.7 kV
Continuous DC collector current, $I_{C,nom}$	1 kA
Maximum operation temperature, $T_{vj,op}$	150 ºC
Rated short circuit current, I_{SC}	4 kA
Gate-emitter maximum voltage, V_{GEs}	+/- 20V
Number of parallel sections	6

 ISBN: 9789075815238 and CFP15850-USB

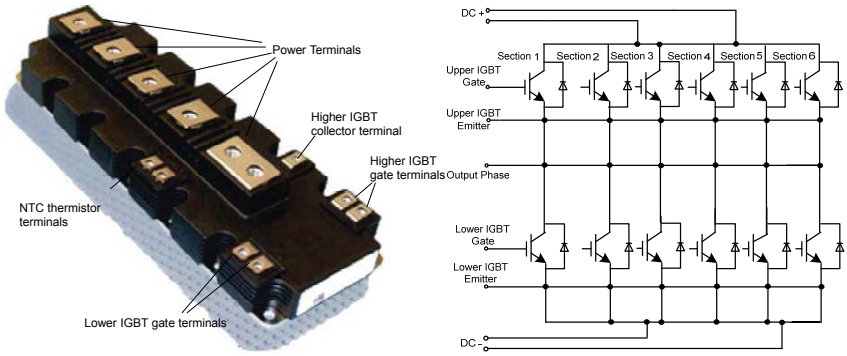


Fig. 1: The IGBT power module under test: (a) the photo of the packaging outline, (b) internal structure of the power module with section definitions.

3. Short Circuit Tests

3.1 Description of the testing setup

During a short circuit, the IGBT module is working in the gate voltage controlled active region, withstanding both high voltage and high current. The corresponding huge power shock (in the range of megawatts) can damage the power module in short transients (i.e., μs-level), and even cause explosions. In order to prevent the potential damages, a state-of-the-art Non-Destructive Tester (NDT) is built up with the current and voltage limits of 6 kA and 1.1 kV, respectively. It can perform repetitive overcurrent and short circuit tests of IGBTs under protected conditions.

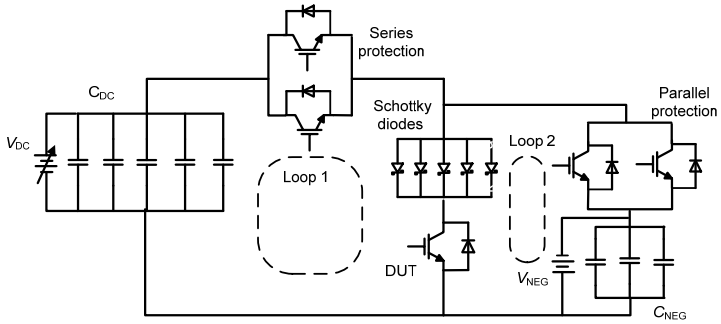


Fig. 2: Circuit schematic of the non-destructive tester.

The basic principle of the non-destructive testing technique is to perform repetitive tests up to the physical limits of the DUT while avoiding device destructions. This characteristic is achieved by some additional protection switches, typically set in series to the DUT. These protection switches are usually IGBT power modules that have higher voltage and current ratings. Fig. 2 shows the principle schematic of the constructed NDT. The NDT structure is described as follows. A high-voltage power supply charges up preliminarily a capacitor bank C_{DC} to a given testing voltage. This capacitor bank supplies all the energy required for the test. A series protection is connected between the capacitor bank and the DUT. It is turned on before the short circuit is activated and switched off right after the short circuit test in order to prevent the DUT from potential explosions. The additional leg in parallel to the DUT contains the parallel protection, a capacitor bank C_{NEG}, and a battery V_{NEG}. The parallel protection has two functions: 1) to assist the series protection during its turn off by diverting the tail current of IGBTs; 2) to act as a crow-bar in case of any instability occurs. The capacitor bank C_{NEG}

and the battery V_{NEG} are used to accelerate the transients. Five Schottky diodes are used to avoid any negative voltage that might be supplied to the DUT. A FPGA supervising unit provides the time control signals for the DUT and protection driving signals with a resolution of 10 ns.

The series protection switch is implemented by 3.3 kV/ 3 kA IGBT modules with a larger physical size compared to that of the DUT, which introduce a considerable stray inductance into the circuit. Two countermeasures are adopted to minimize the overall circuit inductance. First of all, two devices are connected in parallel with optimized placement locations by means of a three-dimensional Computer-Aid Design (CAD) tool. Secondly, the mutual coupling effects are taken into account for the bus bar design. With these considerations, the overall circuit inductance of the Loop 1 shown in Fig. 2 is 37 nH. More details about the NDT can be found in [11].

The short circuit operations can be classified as Type I and Type II [12]: Type I happens at the turn-on of the IGBT. Before turn-on, the gate voltage is negative and the collector-emitter voltage (V_{CE}) is at high level. Immediately after turn-on into short circuit, the collector current increases to several times of the rated current, which is the value of the saturated current at V_{GE}. The IGBT withstands both high voltage and high current, and it should be turned-off within a short duration (i.e., typically less than 10 µs). Type II happens during the IGBT conducting mode. The main difference with Type I is the addition of a transient desaturation phase, which may increase the V_{GE} due to the Miller capacitance and therefore result in a higher short circuit current peak. After the desaturation phase, short circuit current drops to its static value I_{SC}, and the subsequent behavior is the same as Type I. It should be mentioned that Type II short circuit is harsher in converter operations due to the potential oscillations and collector overvoltage. Because Type I short circuit can reflect the semiconductor's performance more directly, this study focuses on the Type I short circuit.

3.2 Experimental results

First of all, a new 1.7 kV/1 kA IGBT module is tested under a 700 V DC voltage for a 10 µs short circuit operation at a room temperature of 25°C. Fig. 3 shows the waveforms of the lower IGBTs collector current I_C, the gate-emitter voltage V_{GE}, and the collector-emitter voltage V_{CE}. It is noted that the peak short circuit current reaches 4.2 kA. The collector voltage drop during short circuit turn-on and voltage peak during short circuit turn-off are related to the effect of the stray inductance and the high current slopes di/dt.

It is worth mentioning that the collector current I_C presents an overshoot and then it decreases with time. This phenomenon is caused by the junction temperature rising during the short circuit [6]. This dynamic electro-thermal coupling phenomenon is well known and has also been simulated for this class of devices by means of a physics-based PSpice-Icepak co-simulation method recently presented in [13].

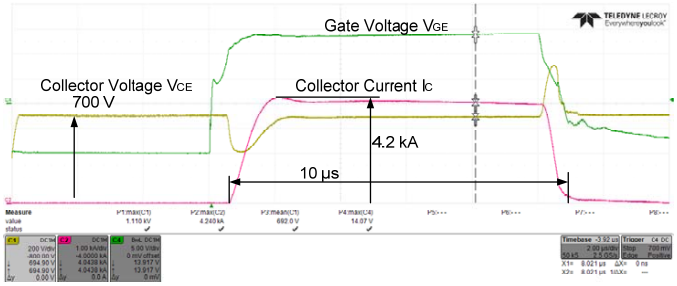


Fig. 3. Experimental waveforms during a 700 V/10 µs short circuit: time 2 µs/div, collector voltage 200 V/div, collector current 1 kA/div, gate voltage 5 V/div.

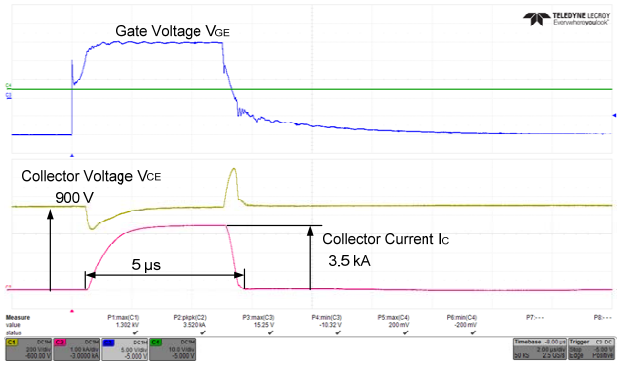


Fig. 4. Experimental waveforms during a 900 V / 5 µs short circuit: time 2 µs/div, collector voltage 200 V/div, collector current 1 kA/div, gate voltage 5 V/div.

Another power module in which the plastic frame and silicone gel have been removed is tested at 900 V DC for a 5 µs short circuit operation. The experimental waveforms of I_C, V_{GE}, and V_{CE} during the short circuit test are shown in Fig. 4. It is worth mentioning that the waveforms refer to the upper IGBTs of the leg. It can be seen that I_C is not obviously decreasing within the 5 µs, which cannot be simply explained by the shorter testing duration. Therefore, further tests on internal current distributions are desirable to study the root-cause mechanism.

The cross-section information of the IGBT module is illustrated in Fig. 5: each IGBT section is connected to the power terminals through copper bus bars. Rogowski coils have been inserted into the bus bars to measure the collector current of each section as shown in Fig. 5. An ultra mini CWT Rogowski probe with a current range up to several kA and a parasitic inductance in the range of a few pH is used for the current measurements [14].

In Fig. 6, the measured short circuit current distribution among the six sections is plotted for the same test of Fig. 4. A mismatched current distribution among the six sections can be observed. It is worth noting that Section 5 and Section 6 have lower *di/dt* during the turn-on transient and the current through them increase with time. On the other hand, Section 2 and Section 3 show an obvious overshoot and their currents decrease with time (same behavior as the I_C in Fig. 3). What above proves that, even though the total current is almost constant during the test, a strong transient imbalance occurs. The above observations imply that the parallel sections may have different stray parameters at the short circuit frequency, which are further studied by detailed simulations in the following section.

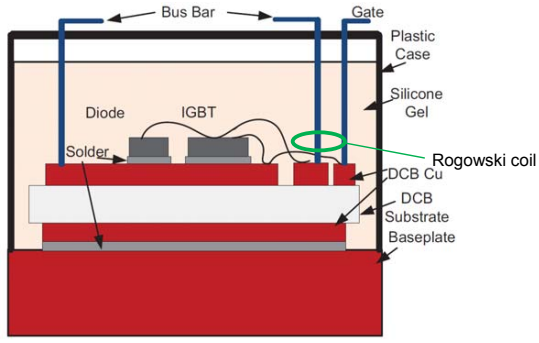


Fig. 5. The cross-section structure of the power module and the Rogowski coil measurement location.

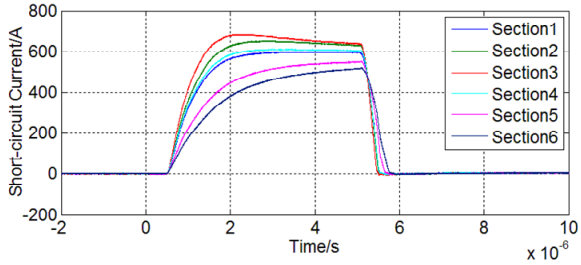


Fig. 6. The experimental waveforms of the collector currents of the six sections under the same condition of the test in Fig. 4.

4. Simulations

PSpice simulations have been performed in this study to further investigate the above observed phenomenon. The procedure is as follows: firstly, the parameters in the PSpice IGBT model are calibrated with the provided information in the DUT datasheet; secondly, an electro-magnetic simulation is performed to extract the stray parameters inside the DUT; thirdly, a circuit profile is defined, which is identical to the executed experiment. The procedure is illustrated in Fig. 7.

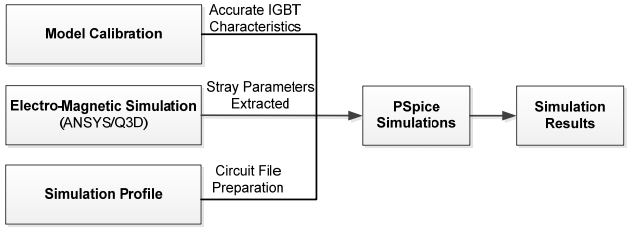


Fig. 7. A schematic of the simulation procedure.

4.1 Model calibration

A physics-based lumped-charge IGBT Spice model [15] is used, which has been proved to have a higher accuracy for high voltage IGBTs with respect to the embedded PSpice IGBT model. Based on the datasheet information, the IGBT model has been calibrated at different conditions. The IGBT model output characteristics at different V_{GE} (i.e., 8 V, 10 V, and 15V) are plotted in Fig. 8, which are also compared with the curves in the datasheet of the DUT.

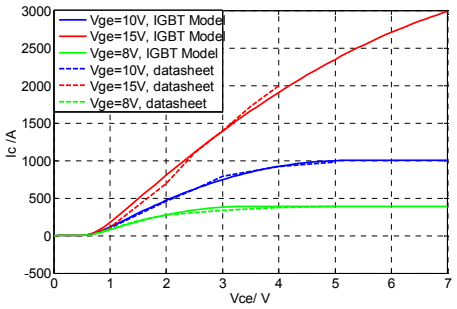


Fig. 8. The output characteristics based on the obtained PSpice IGBT model and the datasheet.

4.2 Electro-magnetic simulation

A detailed discussion on the stray parameters extraction of the DUT has been presented in a recent study [15]. A brief introduction is given as follows. First, a detailed geometry is created in a CAD program and further imported to the software ANSYS/Q3D. Then, Q3D applies Finite-Element Method (FEM) to extract the matrices of resistance, inductance, and capacitance. Simulations are performed in Q3D at a specific frequency. The corresponding stray inductances and stray resistances of the six sections (from the power terminals to each section) are extracted. The simulations are done in such a way that, when extracting the inductance and resistance of a certain section, only the IGBT chip of this section conducts. It is worth noting that simulations should be performed at each specific frequency individually instead of by using the "frequency sweep" available in Q3D. It is because that the finite element mesh for the adaptive solution is optimized for the simulated frequency only, and the accuracy of the results could vary significantly at frequencies different from the specified frequency. The simulated stray inductances and stray resistances of different sections at 100 kHz (i.e., corresponding to a 10 µs transient) are listed in Table II. The results show that the middle sections (Sections 2-4) have lower stray inductances and stray resistances than the other sections.

Table II: The stray parameters of each section at 100 kHz.

	Section 1	Section 2	Section 3	Section 4	Section 5	Section 6
Stray resistance (µΩ)	1449	850	469	665	931	1559
Stray inductance (nH)	70	43	33	44	62	82

4.3 Simulation results

With the calibrated IGBT model and the extracted stray parameters, PSpice simulations are performed under the same conditions as the experiments: a DC voltage of 900 V DC, a short circuit duration of 5 µs, and at the room temperature of 25°C. The PSpice simulation circuit is plotted in Fig. 9. $L_{circuit}$ represents the circuit stray inductance, while R_{xm}, L_{xm} (m = 1, 2,…, 6) represent the stray parameters of the six sections. The simulation results of the I_C and V_{CE} are plotted as dashed lines in Fig.10 (a), which are compared with the experimental waveforms of Fig. 4 (shown in solid lines). The simulation results of the short circuit currents in each section is shown in Fig. 10(b) in dashed lines, compared with the corresponding experimental results in solid lines.

In Fig. 10(a), the PSpice simulated waveforms coincide with the experimental ones: I_C behaves similar rising slopes, and V_{CE} have same voltage undershoot/overshoot transients during short circuits. It is noted that the simulated short circuit current is slightly higher than the experimental one in Fig. 10(a). This is because the PSpice simulations are performed at a constant temperature of 25°C. While in the experiments, the IGBT chip temperature increases to a much higher temperature during the short circuit operation. The short circuit current is reduced with the increase of the chip temperature. It suggests that further simulations dealing with the IGBT dynamic electro-thermal coupling effects at µs-level is demanded to achieve a more accurate prediction of the short circuit performance.

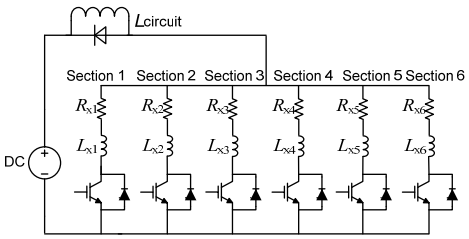
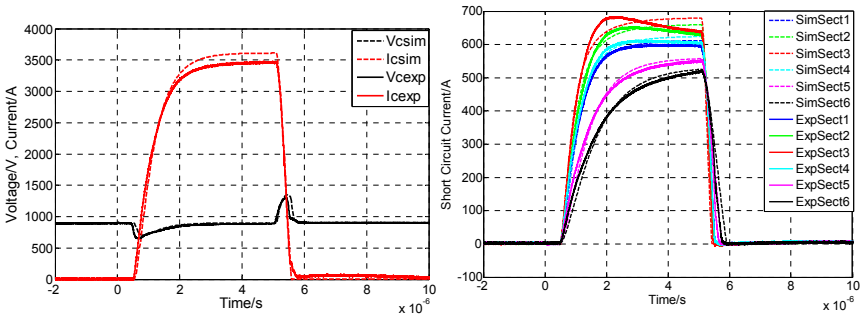


Fig. 9. The PSpice circuit for simulating the current distributions during short circuits.



(a) (b)

Fig. 10. The PSpice simulation results: (a) the whole module short circuit waveforms, comparing with experimental waveforms in Fig. 4; (b) simulated section currents, comparing with waveforms in Fig.6.

In Fig. 10(b), the PSpice simulated *di/dt* coincides with the experiments. This comparison confirms the differences in stray parameters among the parallel sections. The middle sections (Sections 2 and 3) have higher *di*/*dt* and carry higher currents, while the farthest sections (Sections 5 and 6) have lower *di*/*dt* and conduct lower current. Meanwhile, due to the aforementioned dynamic electro-thermal coupling effects, the currents of Sections 2 and 3 visibly show overshoots and decrease with the operation time. Because of the higher inductances, the Sections 5 and 6 currents increase during the entire operation time. It is worth noting, though, that the current differences tend to reduce at the end of the short circuit, evidencing a dominating effect of the inductance in the imbalance phenomenon. From Fig. 6 and 10(b), it is observed that Sections 2 and 3 have higher current stresses which may fail faster than other sections.

In order to study the impact of the stray parameters on the internal current distribution, a further PSpice simulation is performed with a set of assumed stray parameters with reduced differences among the six sections. The stray parameters of Sections 5 and 6 are within 1.5 times the values of Sections 2 and 3. The simulation is done under the same conditions as simulation presented above. The simulated short circuit current waveforms are plotted in Fig. 11. The current imbalance is within 50 A (i.e., less than 10%) among the six sections. This suggests the current imbalance phenomenon can be minimized by decreasing the stray parameters imbalance.

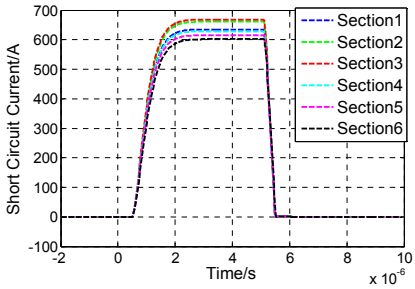


Fig. 11. The simulation results of the short circuit section currents under a set of assumed stray parameters with reduced differences among different sections.

5. Conclusion

This paper investigates the short circuit performance of the MW-level IGBT power module by means of experiments and simulations. It has been shown that the stray parameters imbalance lead eventually to a non-equal current distribution among the parallel chips. Both simulations and experiments show that some chips are more stressed than others during short circuits, as well as suggest a dominating effect of the inductance in the imbalance phenomenon. The proposed study can provide a feedback to module designers on optimizing module's internal structure and geometry, as well as give suggestions for application engineers to improve the thermal management and/or cooling system design.

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